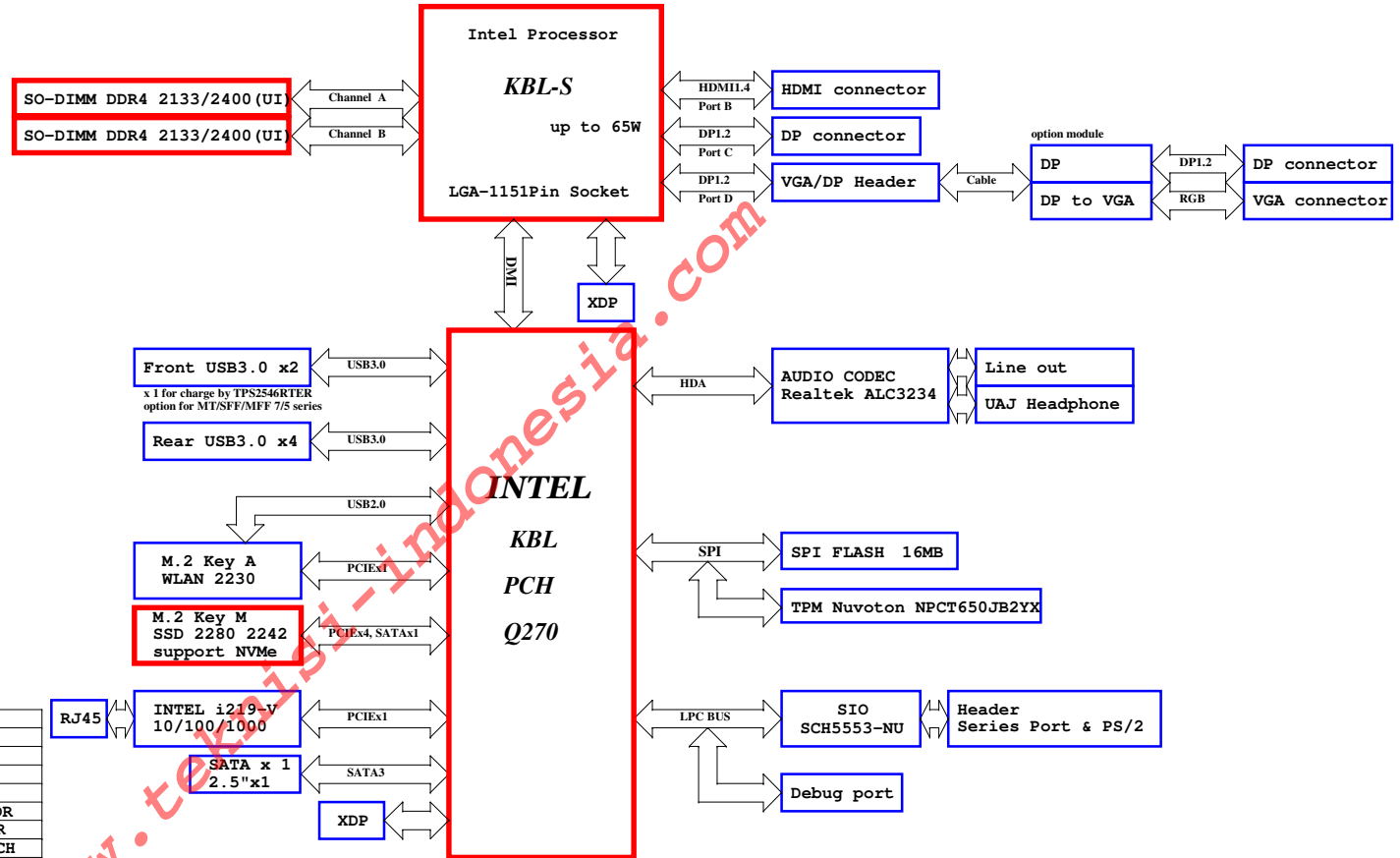


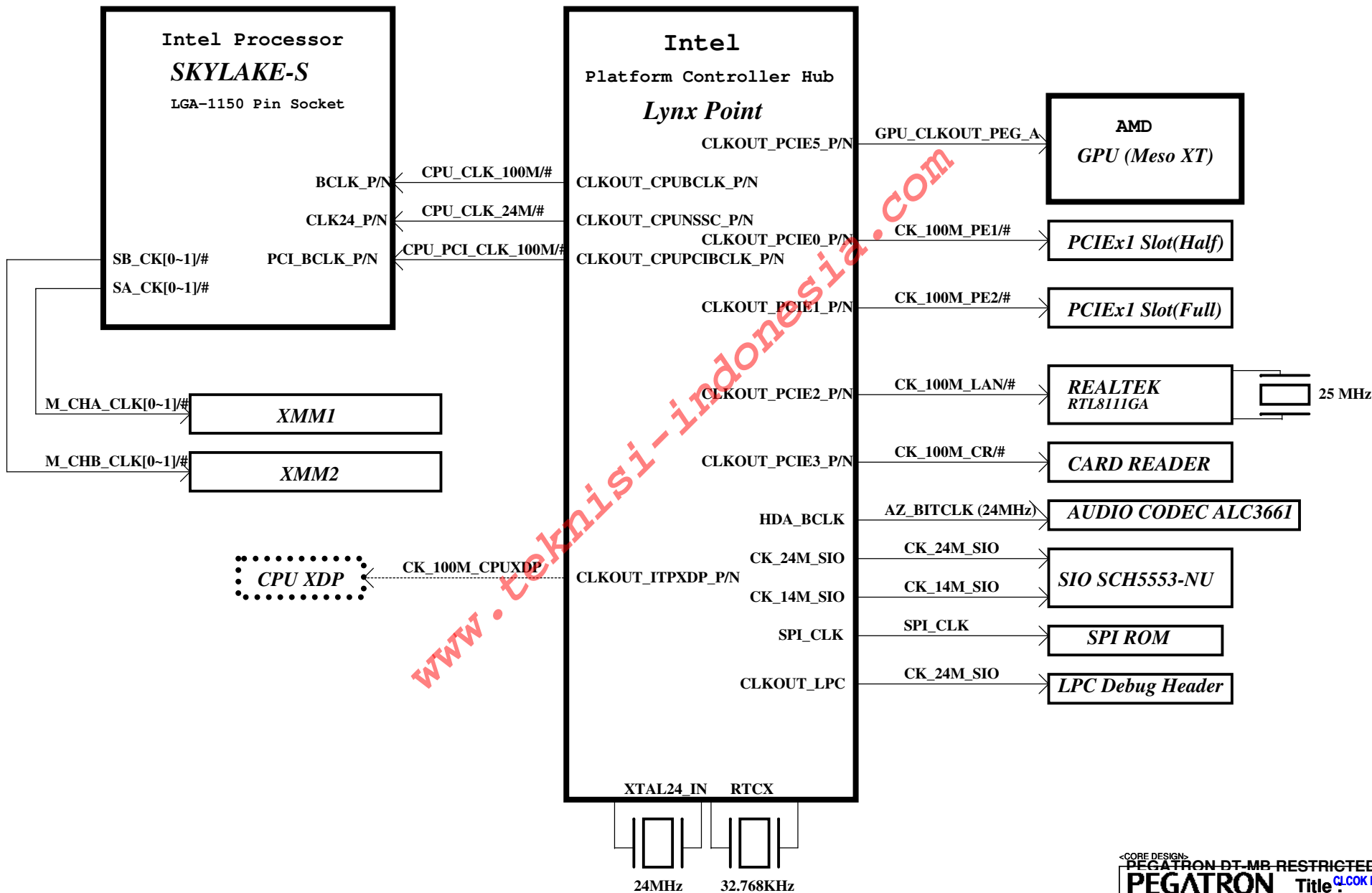
Revision: A00

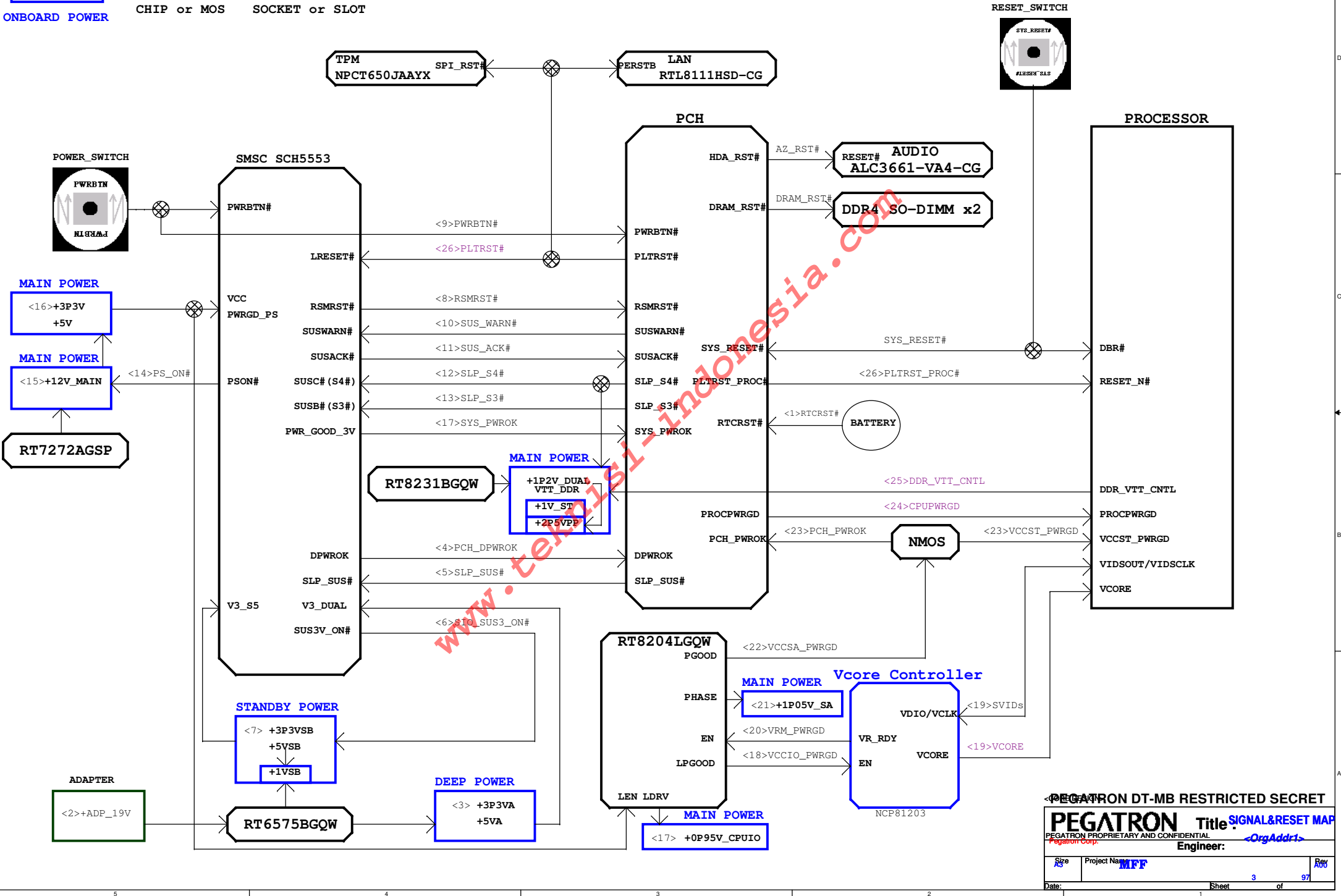
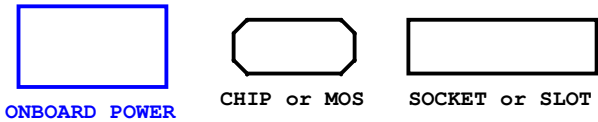
PAGE	TITLE
01	BLOCK DIAGRAM
02	CLOCKS DISTRIBUTION
03	SIGNAL & RESET MAP
04	CHANGE HISTORY
05	POWER FLOW 35W
06	POWER DISTRIBUTION
07	POWER SEQUENCE
08~13	CPU LGA1151
14	DDR4 SODIMM CH-A
15	DDR4 SODIMM CH-B
16	DDR4 TERMINATION A&B
17~24	INTEL PCH
25	SM BUS Control
26	SPI ROM
27	ME DISABLE
28	NGFF KEY A 2230 (WLAN)
29	NGFF KEY M 2280 (SSD)
30	LOM Intel i219
31	LAN JACK
32	N/A
33	Front USB3.0
34	N/A
35	Front 3.0 USB CHARGE IC
36	REAR USB3.0
37	REAR USB3.0
38	N/A
39	TYPEC CYPD2122
40	TYPEC CONN
41	PS2 and Comport header
42	VGA option header
43	REAR LINE OUT& GHS CONN
44	N/A
45	SIO SCH5555V-NU
46	SCREW HOLE
47	FAN CIRCUIT
48	intruder
49	DEBUG LED
50	APS/LPC DEBUG
51	RTC
52	SATA HDD CONN & LED
53	HDMI OUT
54	AUDIO CODEC ALC3234
55	PWRBTN & LED
56	N/A
57	N/A
58	TPM Z32H320TC
59	TPM NPCT650JAAYX
60	DP CONN
63~64	DC IN
65	PCHPWROK_VCCSTPG
68	VCCSA & VCCIO
69	5VSB/+5VA/+3P3VA
70	+3P3VSB/WLAN



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title: BLOCK DIAGRAM	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Pegatron Corp.		Engineer: <OrgAddrs>	
Size K2	Project Name MFF	1	97
Date:		Sheet	of

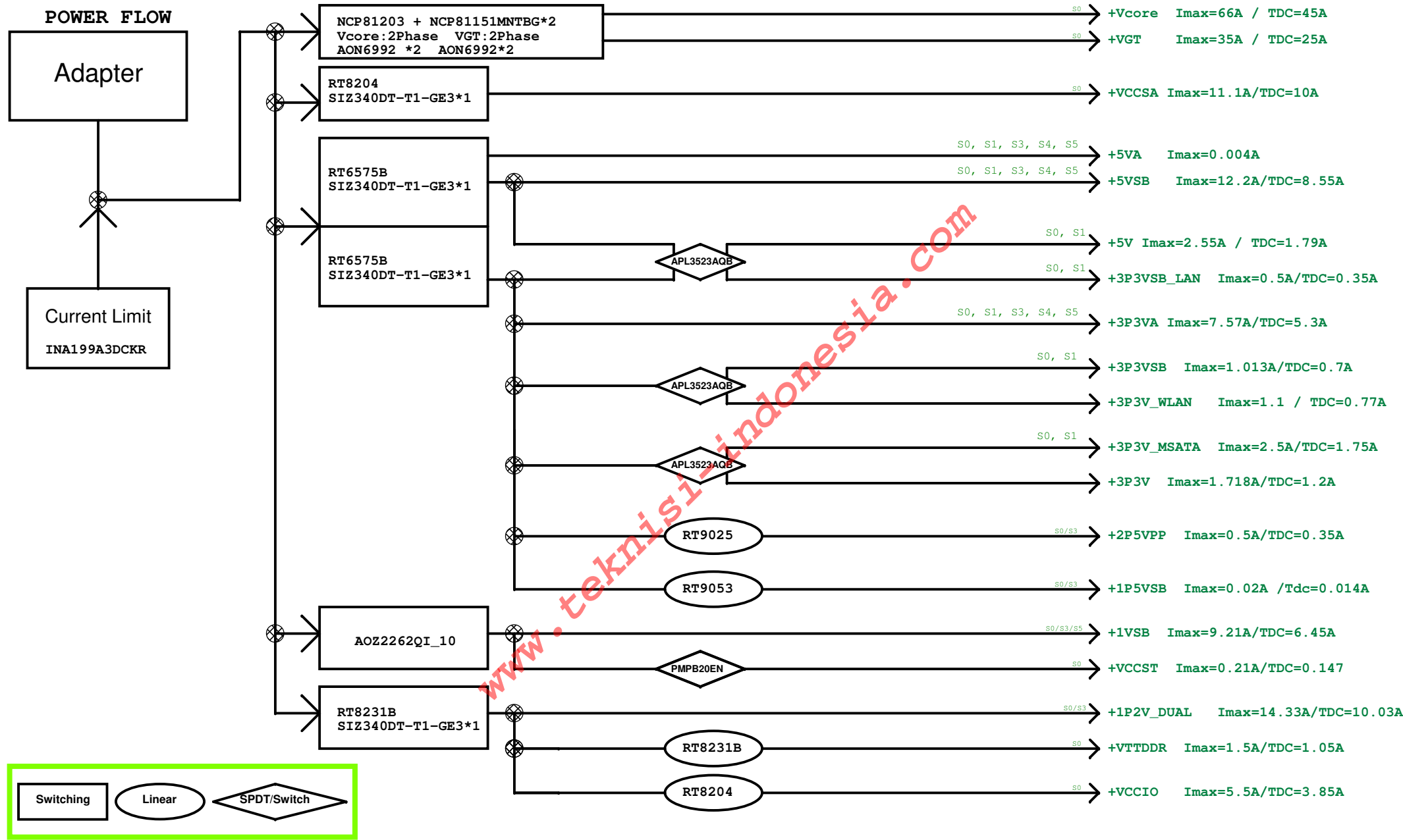




Schematics Change History

[illegible]

```
e C power switch (UU60) enable issue
all AP29 (RSVD17)
from PCH GPP_B20 to GPP_E0
r R935 for CCG2 SMBUS address select
```



<CORE DESIGN>

PEGATRON		Title : POWER FLOW	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Pegatron Corp.		Engineer: <OrgAddr1>	
Size A3	Project Name MFF	Rev A00	
Date:		Sheet 5	of 97

+VCORE
+1P05V_SA (+VCCSA)
+V_GT (+VCCGT)
+0P95V_CPUIO (+VCCIO)
+1V_ST (+VCCST)
+1P2V_DUAL (VDDQ)
VCCST_PWRGD (VCCSTG)

CPU SKYLAKE-S	
-> 70A - 65W	
-> 11. 1A	
-> 35A	
-> 5. 5A	
-> 0. 06A+0. 15A	
-> 2. 8A+0. 13A	
-> 0. 02A	

+1VSB
+3P3V
+3P3VSB
+3P3VA
+BATT

PCH Lynx Point	
-> 7. 11A	
-> 0. 007A	
-> 0. 74A	
-> 0. 2A	
-> 0. 001A	

+1P2V_DUAL
+VTT_DDR

DDR4	
-> 9. 51A	
-> 0. 75A	

+3P3V
+3P3V
+5V_LCD

Panel (HD)	
eDP to LVDS IC (S1U1)-> 2A	
eDP to LVDS EEPROM (S1U2)-> 0. 003A	
-> 1. 2A	

+3P3V

DP	
DP Conn (125)-> 0. 5A	

+3P3V

+5V_HDMI

HDMI	
HDMI-Redriver (MU1)-> 0. 2A	
HDMI-Out Conn (J137)-> 0. 5A	

+3P3VSB_LAN

LAN IC	
LAN IC (LU1)-> 0. 3A	

+3V_WLAN

WLAN	
WLAN (J218)-> 2A	

+3P3V

M. 2	
M. 2 (J1)-> 2. 5A	

+3P3VSB

CR_3V3

CARD READER	
CR IC (U3)-> 1. 6A - 5. 28W	
CR CONN (J2)-> 0. 8A-2. 64 W	

+3P3VSB

+5VSB

+3P3V

ALC3224 Codec	
-> 12mA - 39. 6mW	
-> mA	
-> 12mA - 39. 6mW	

+5V_FAN

CPU FAN (P70)	
-> 0. 9A -8. 4 W	

+5VSB

ODD & HDD	
HDD-> 1A - 5W	
ODD-> 2A - 10W	

+5VSB

+5VSB_CHARGING

+5VDUAL_WAKE

+5VDUAL_WAKE

+5VDUAL_WAKE

USB PORTS	
Charge IC -> 2. 5A	
SIDE USB3.0 (J221) -> 2A	
SIDE USB3.0 (J212) -> 0. 9A	
REAR USB3.0 x2 (J226) -> 1. 8A	
REAR USB2.0 x2 (J210) -> 1A	

+3P3VSB

WEBCAM	
-> 0. 5A	

+5VDUAL_WAKE

TOUCH	
-> 0. 5A	

+3P3V

+3P3VA

+3P3VSB

+BATT

SIO SMSC5555	
-> 1mA - 3. 3mW	
-> 11mA - 36. 3mW	
-> 500mA - 1. 65W	
-> 1mA - mW	

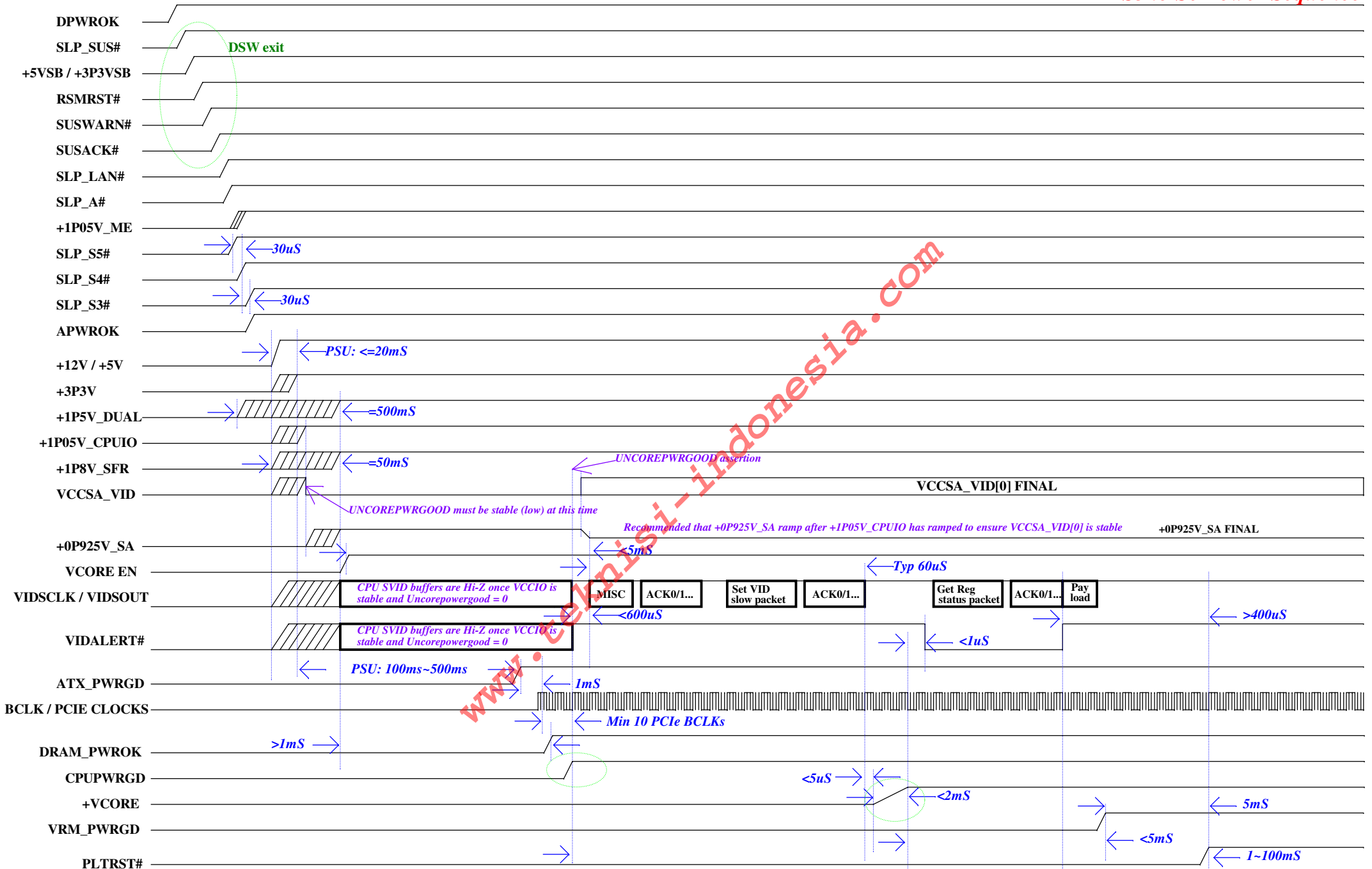
+3P3V

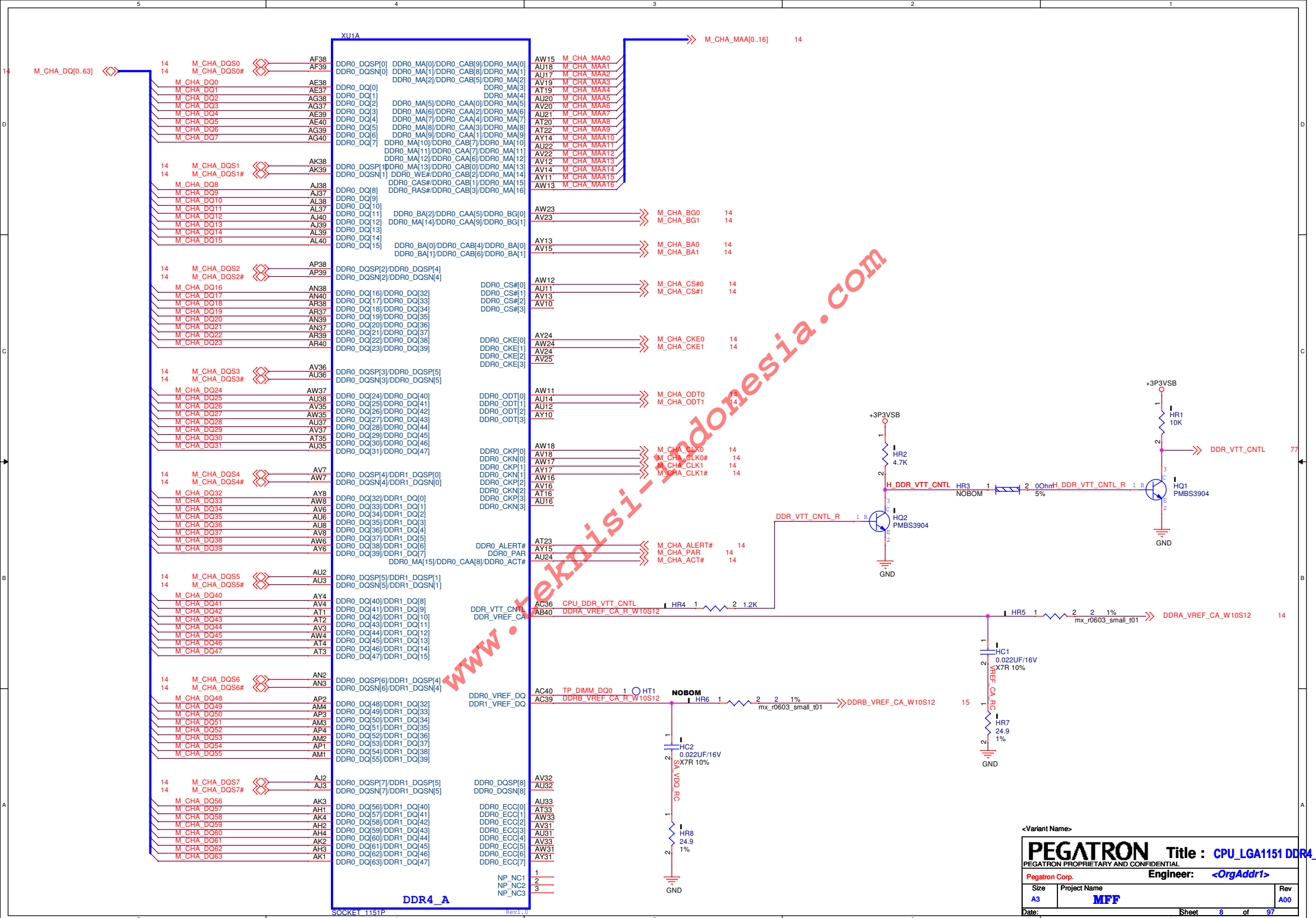
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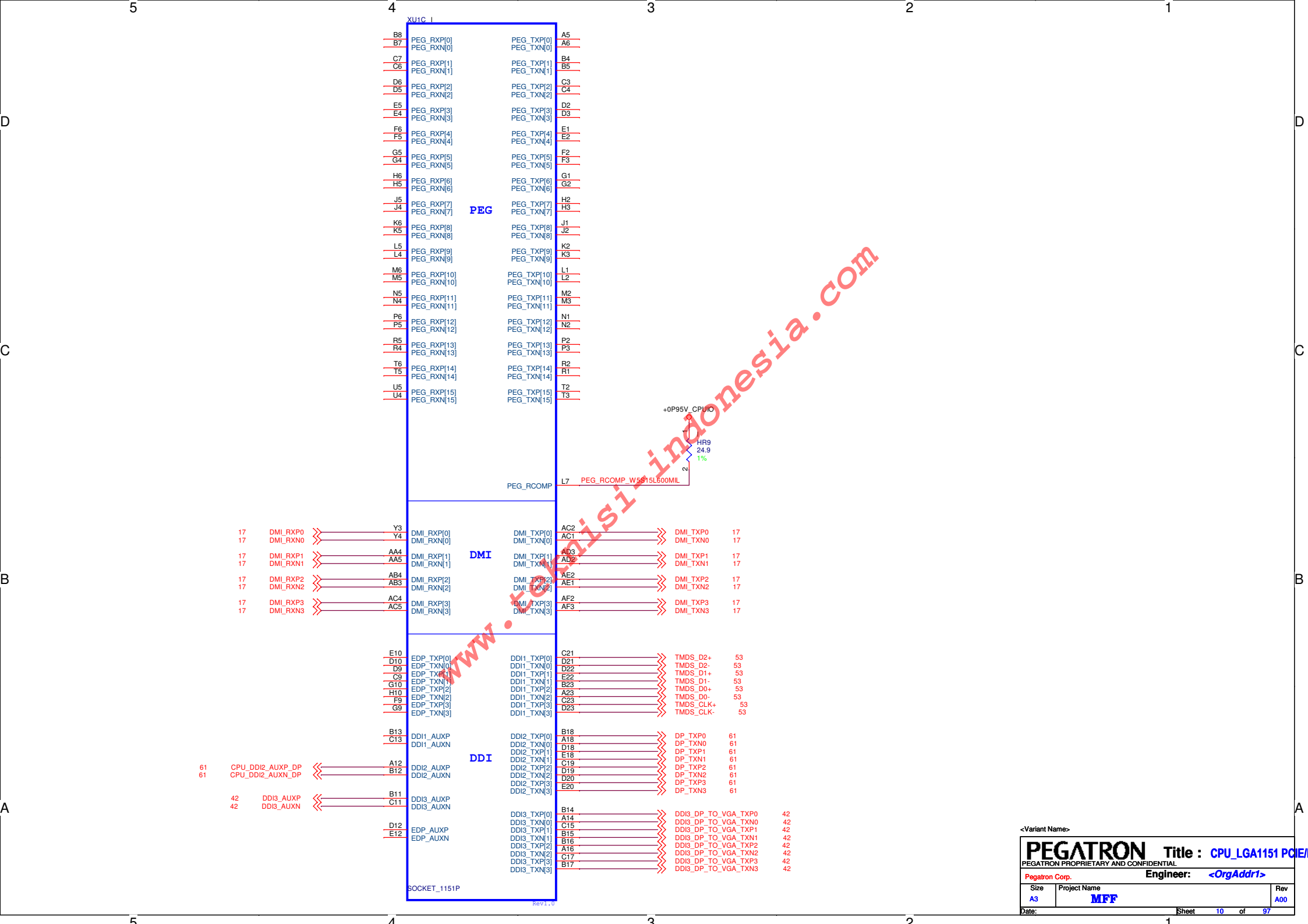
TPM	
TPM-> 1mA	
TPM-> 0. 3A	

+3P3VSB

SPI	
-> 50mA - 165mW	







<Variant Name>

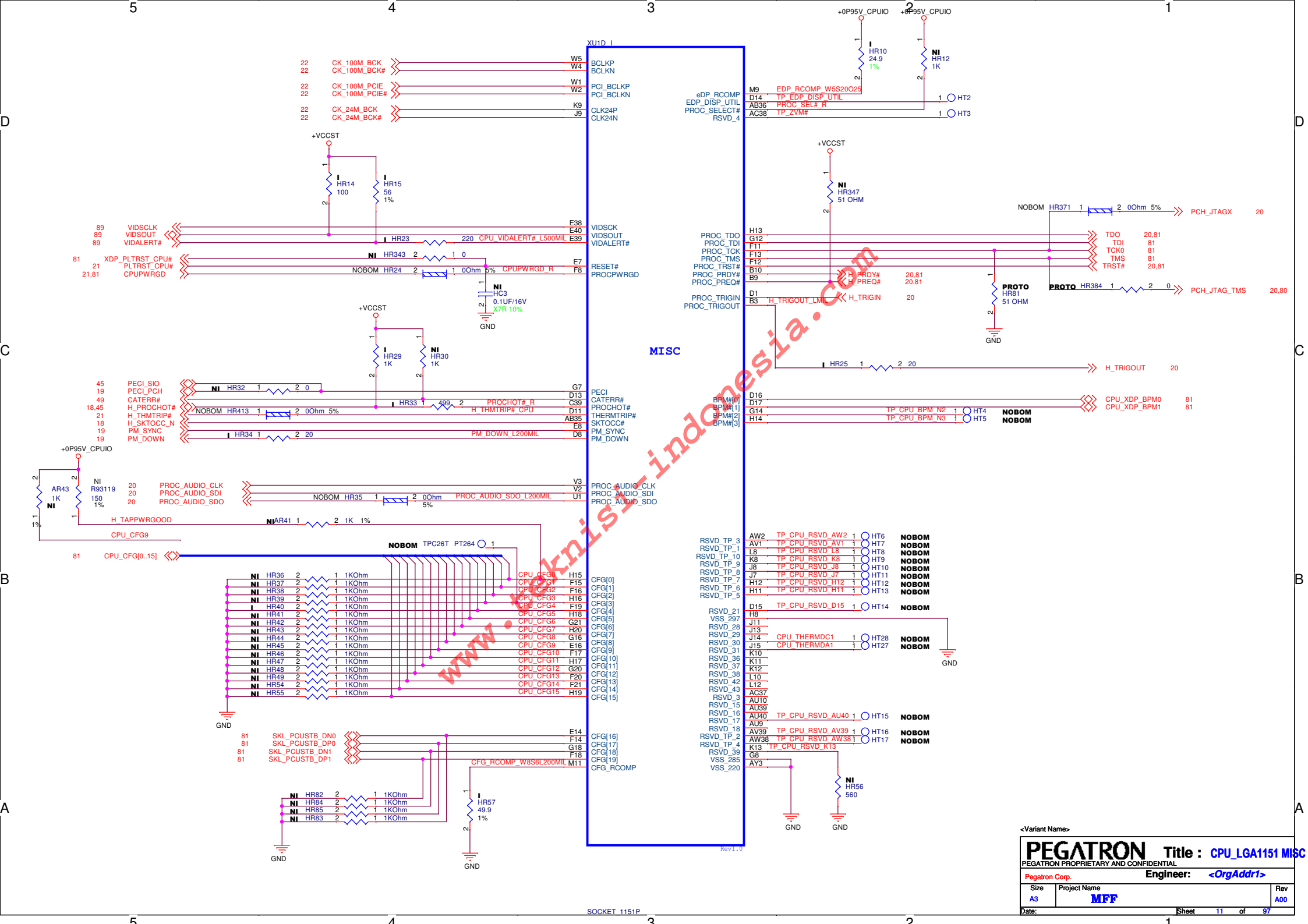
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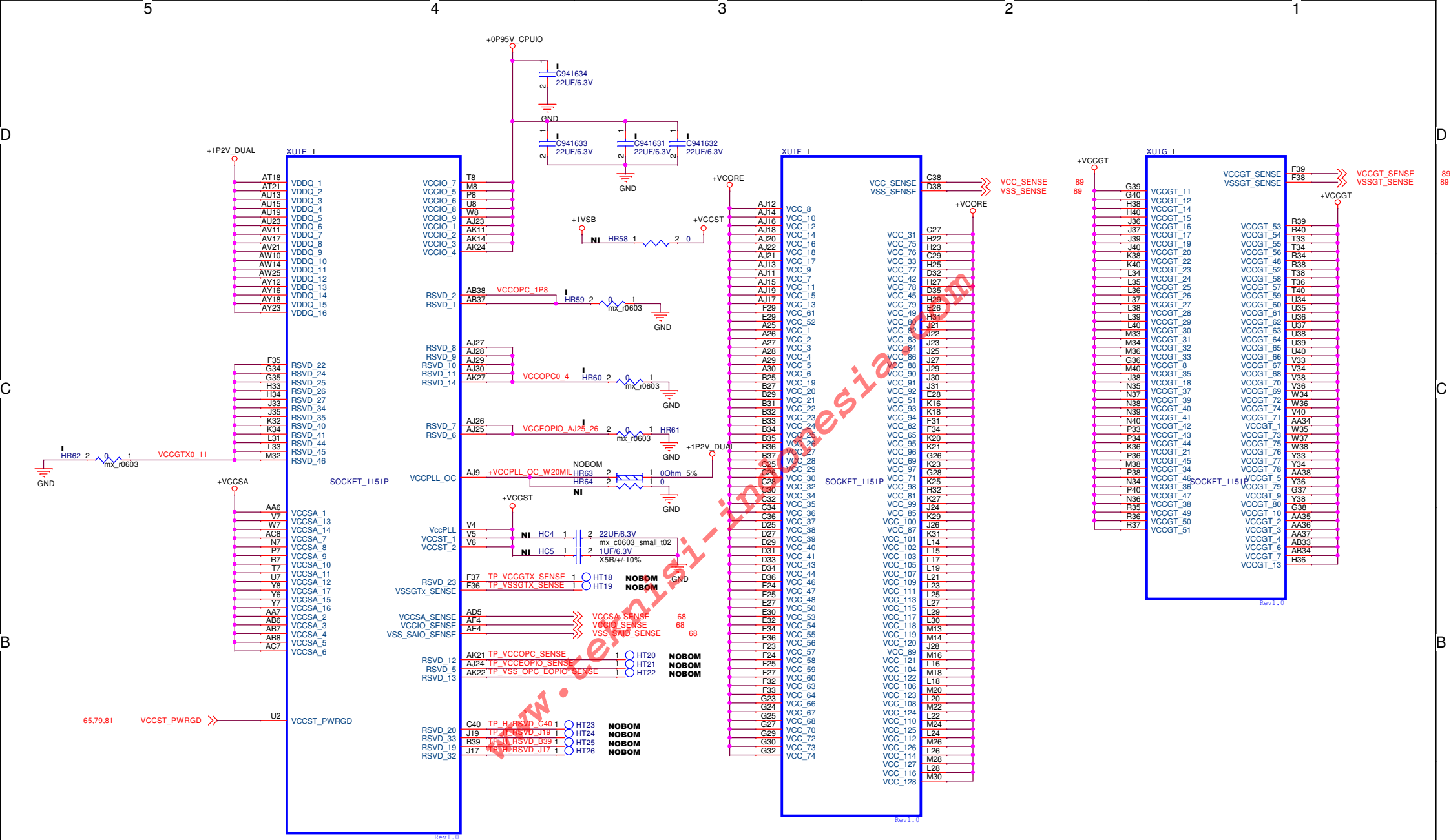
PEGATRON PROPRIETARY AND CONFIDENTIAL

Pegatron Corp. Engineer: <OrgAddr1>

Size A3 Project Name MFF Rev A00

Date: Sheet 10 of 97





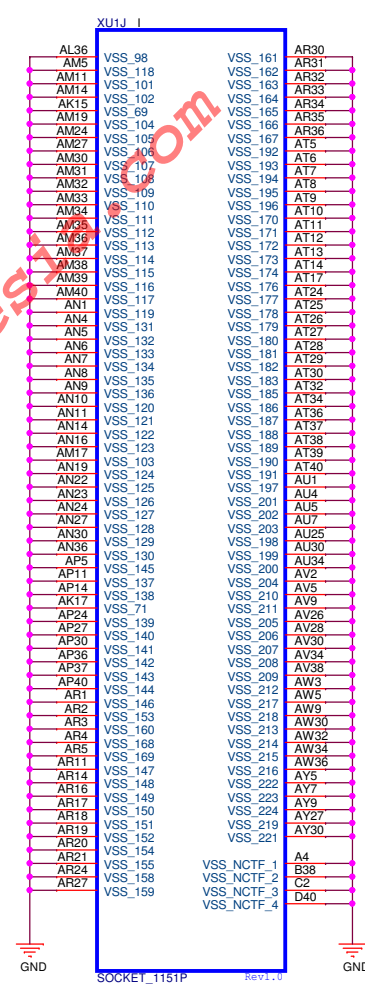
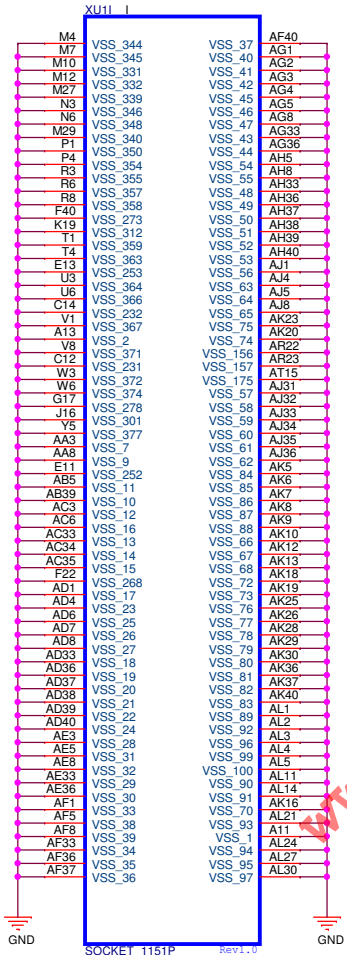
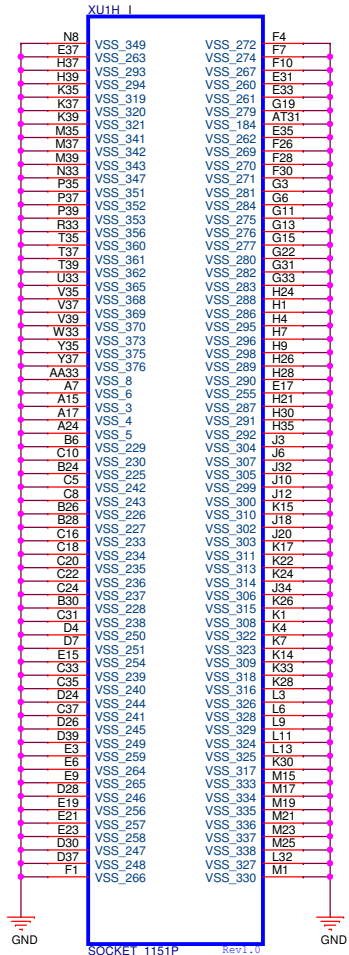
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PEGATRON Title : CPU_LGA_1151_VCC
PEGATRON PROPRIETARY AND CONFIDENTIAL

Pegatron Corp. Engineer: <OrgAddr1>

Size	Project Name	Rev
A3	MFF	A00

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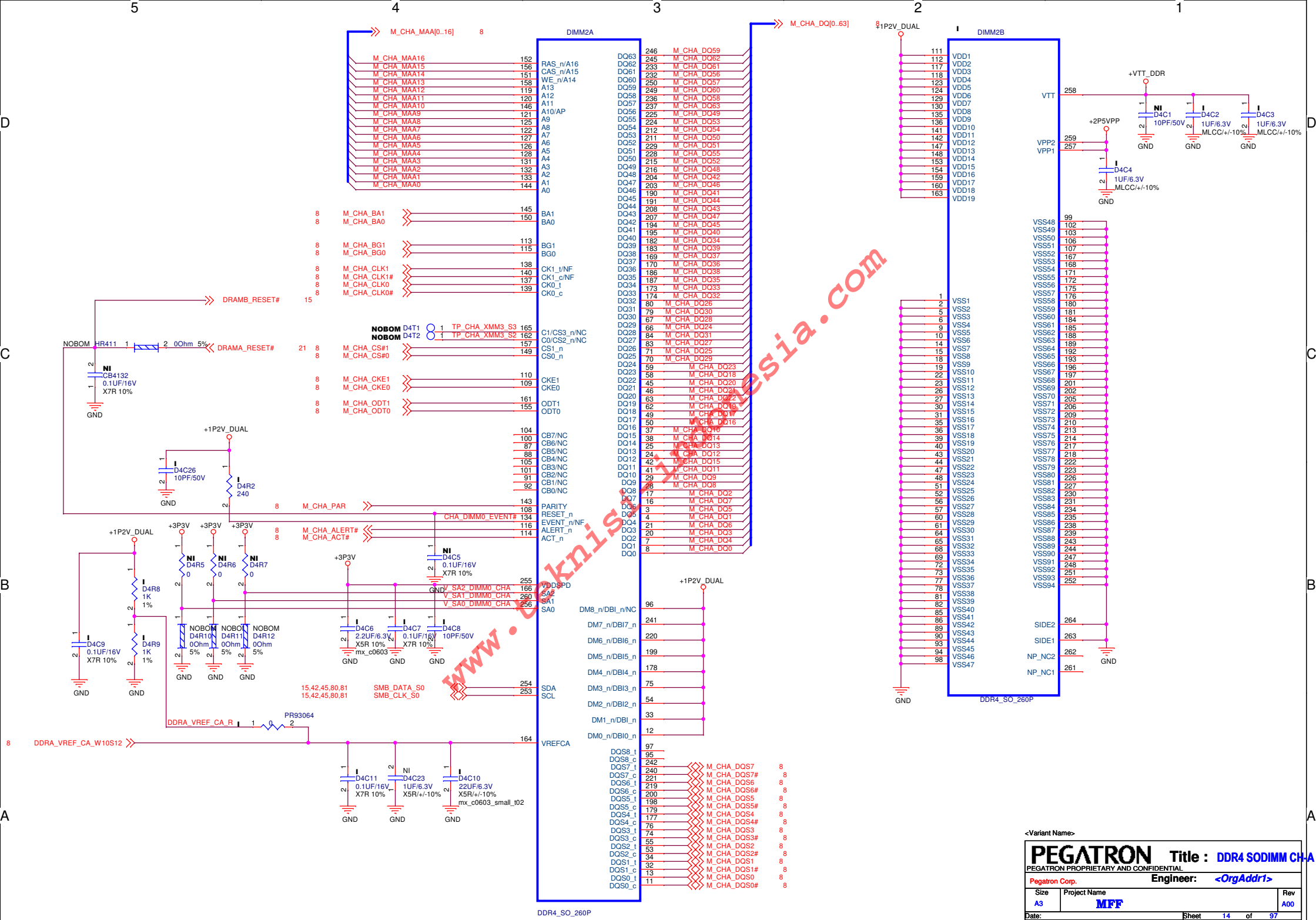
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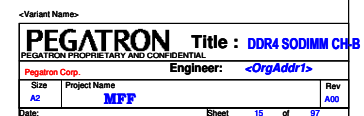
PEGATRON Title : CPU_LGA_1151 VSS
PEGATRON PROPRIETARY AND CONFIDENTIAL

Pegatron Corp. Engineer: <OrgAddr1>

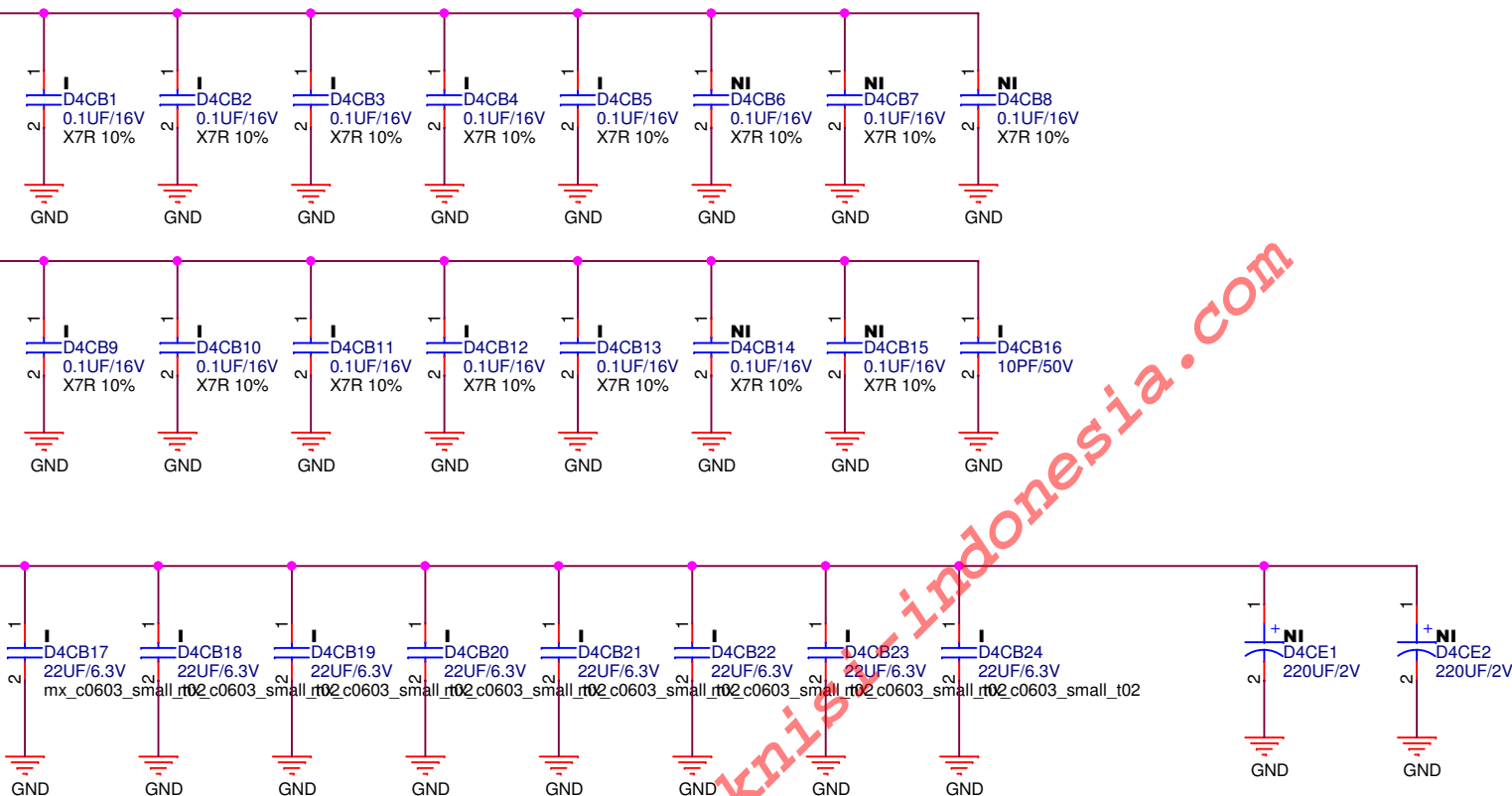
Size	Project Name	Rev
A3	MFF	A00

Date: Sheet 13 of 97



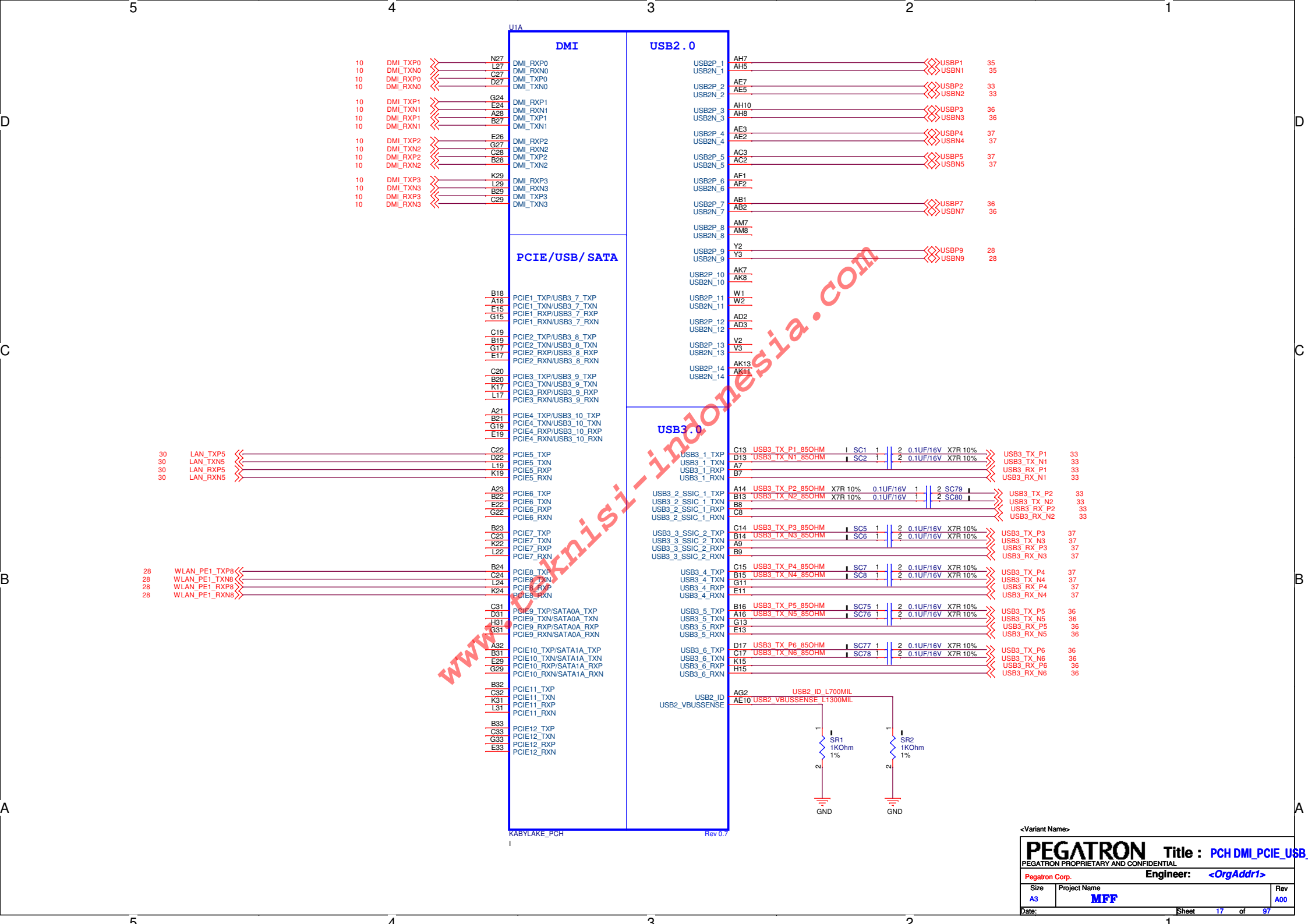


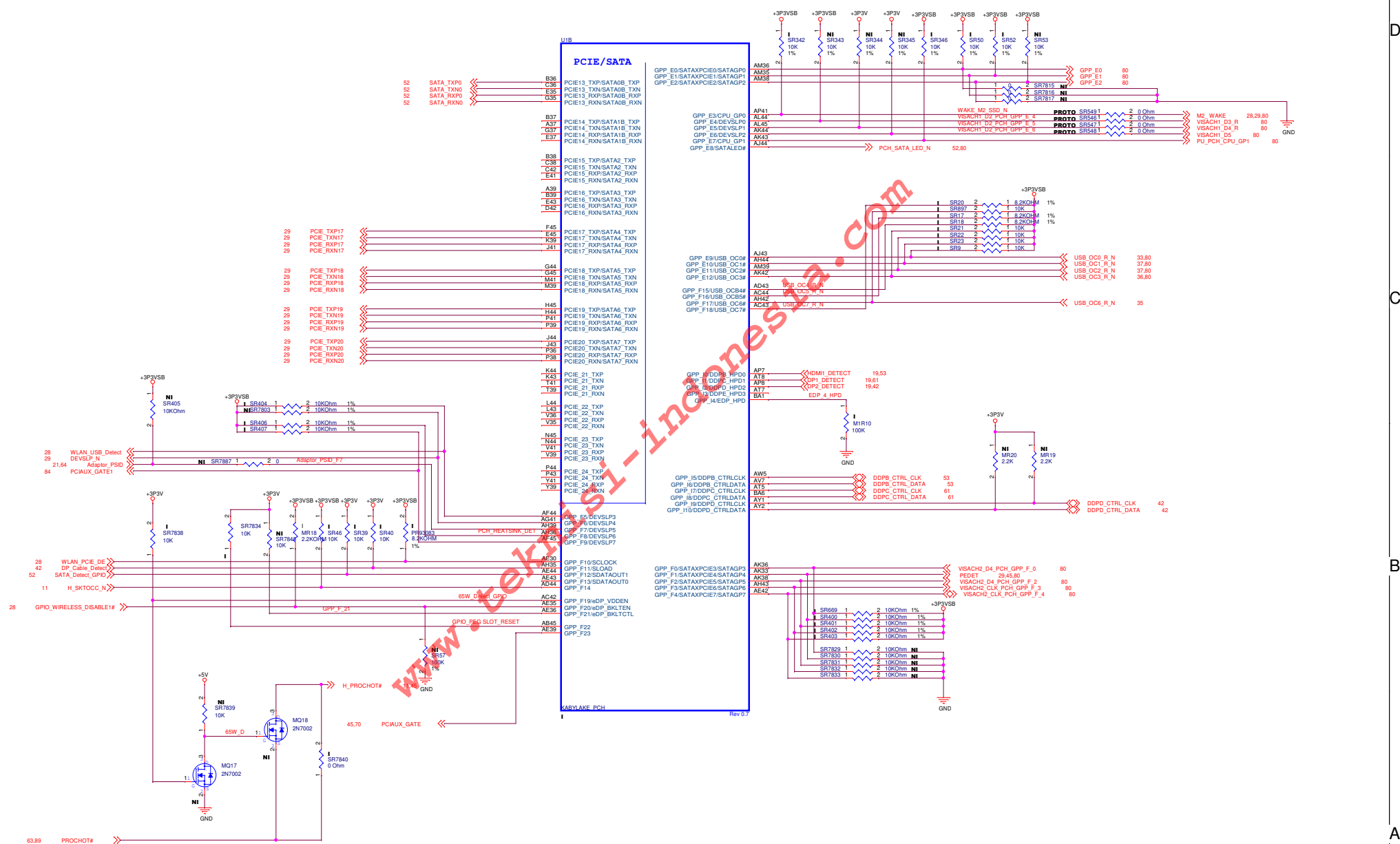
+1P2V_DUAL

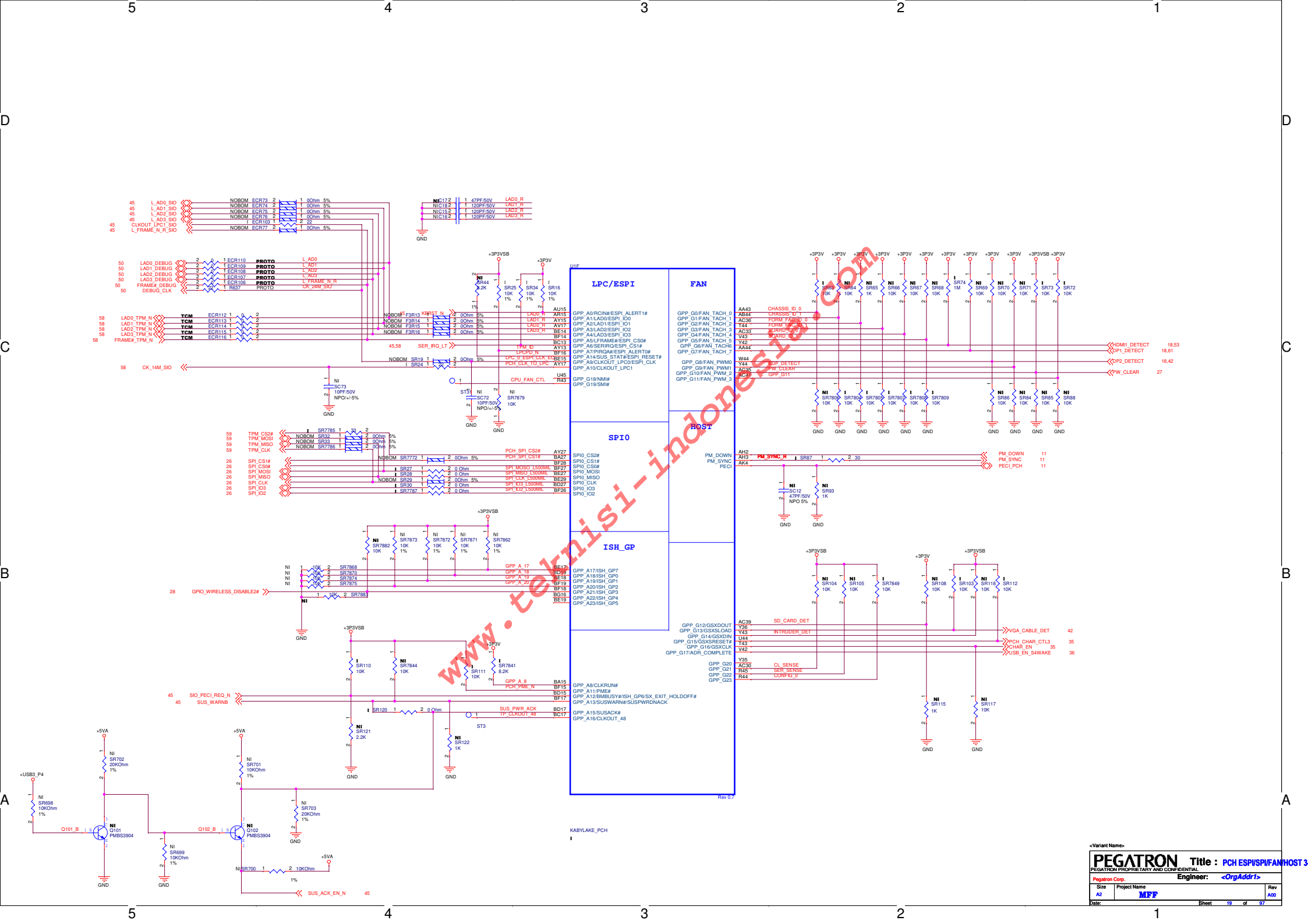


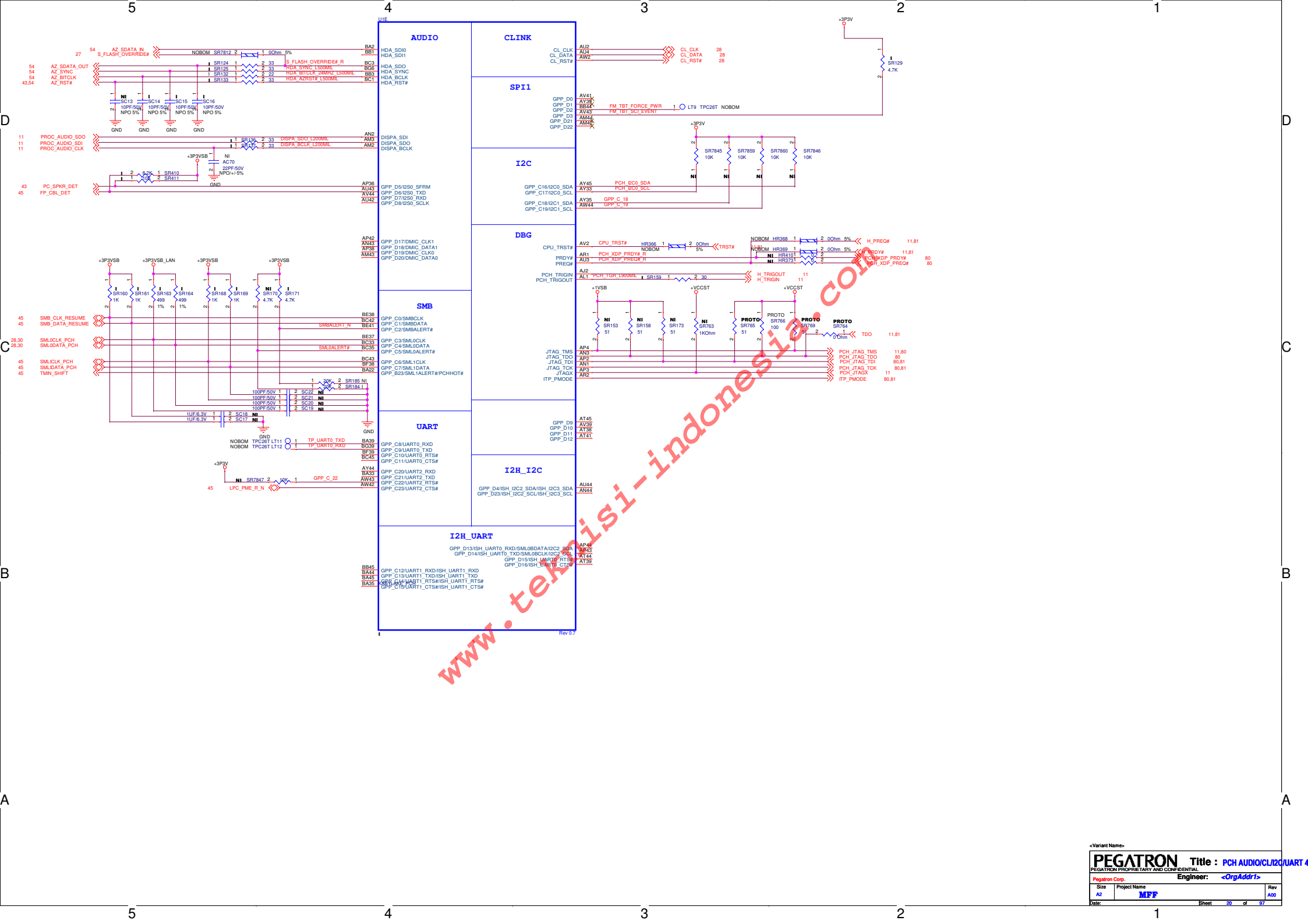
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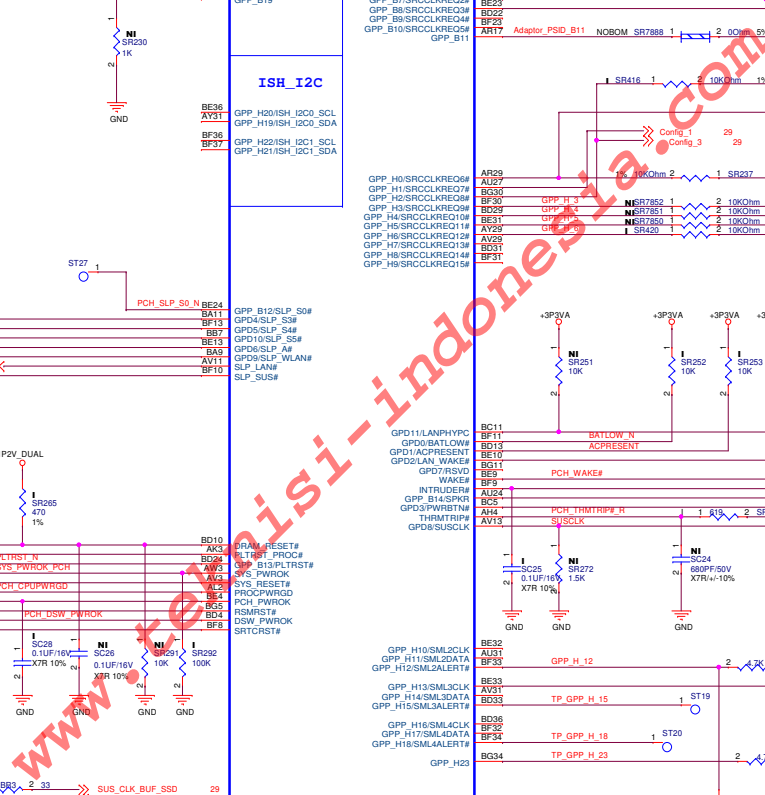
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Pegatron Corp.		Engineer: <OrgAddr1>	
Size	Project Name		Rev
A4	MFF		A00
Date:	Sheet 16 of 97		

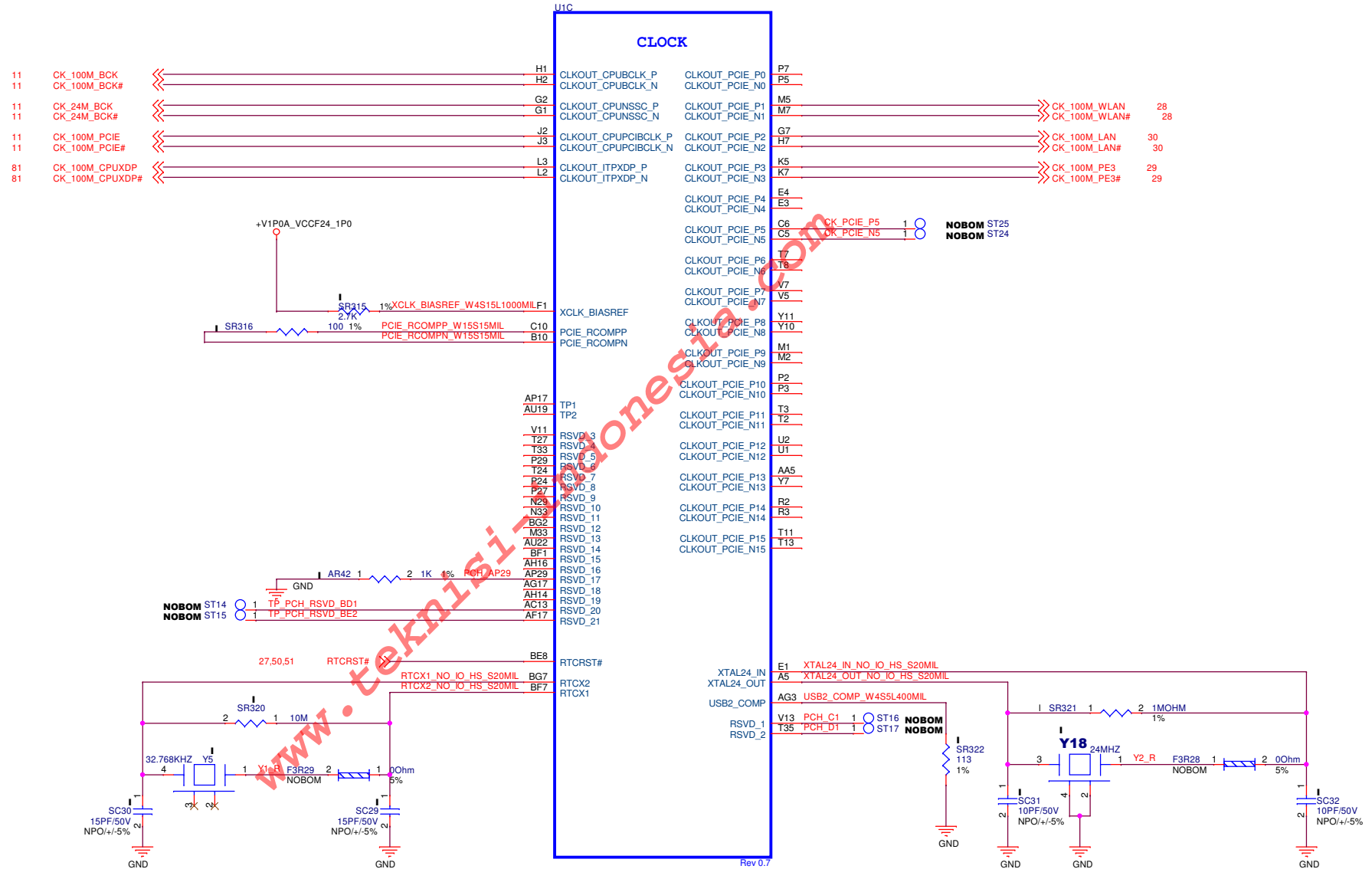












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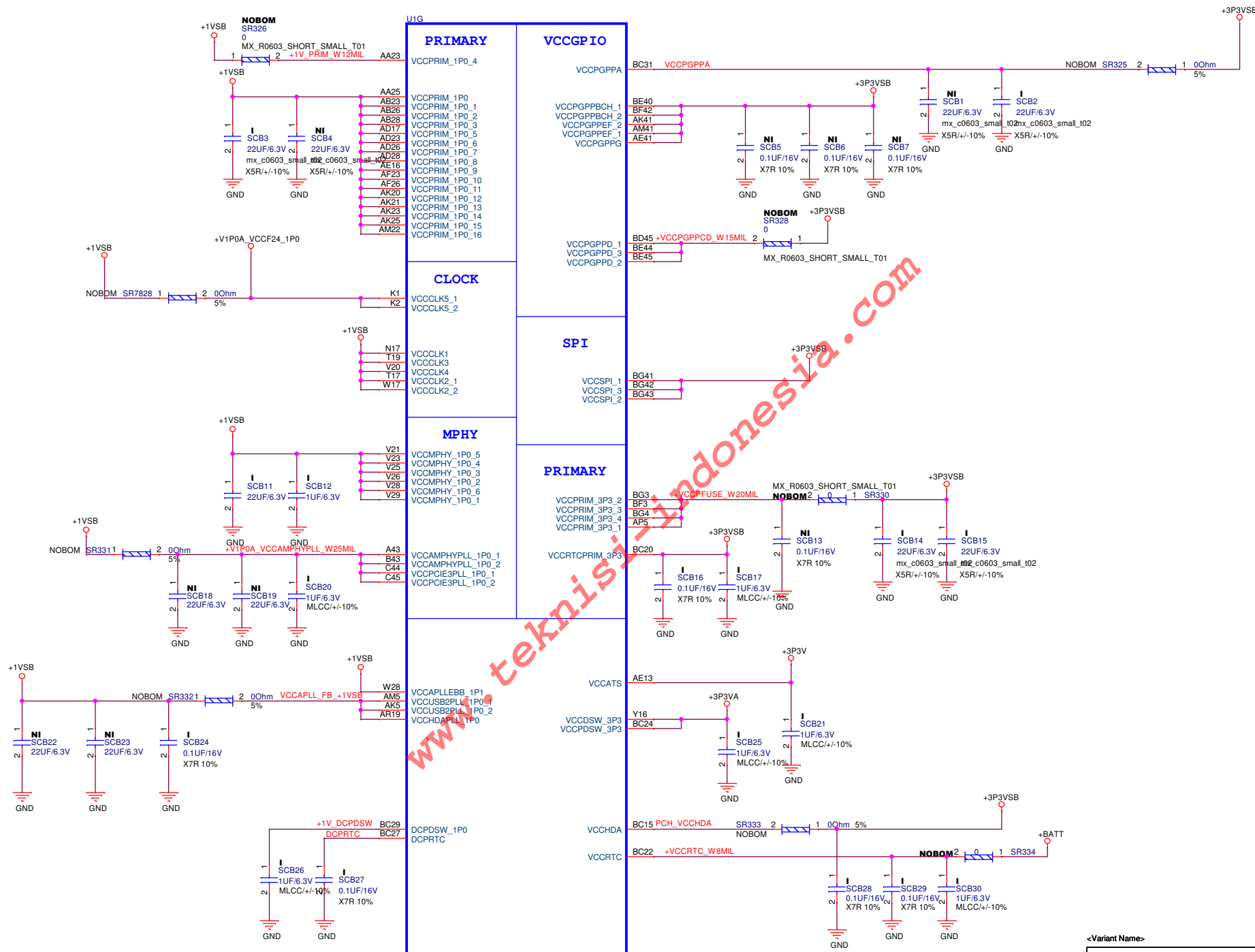
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PEGATRON PROPRIETARY AND CONFIDENTIAL

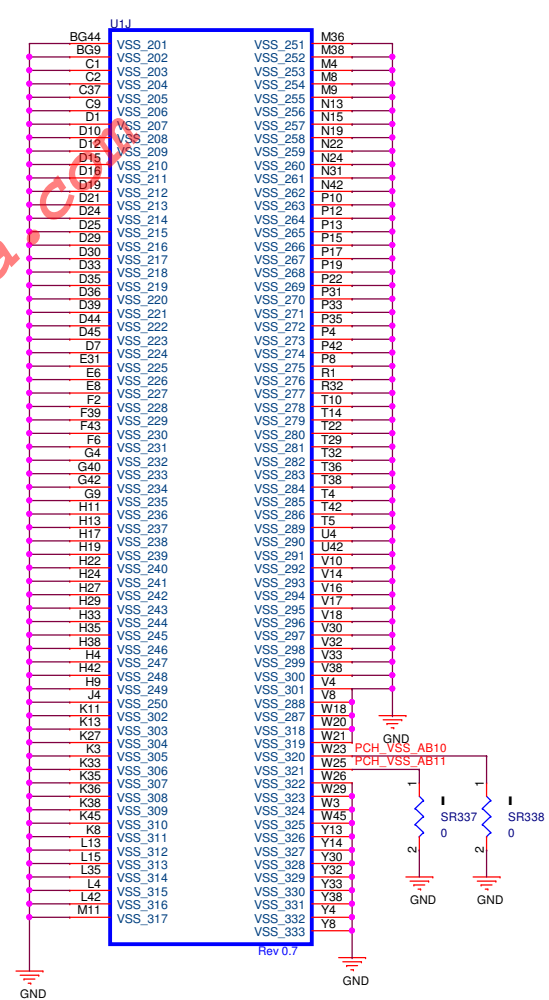
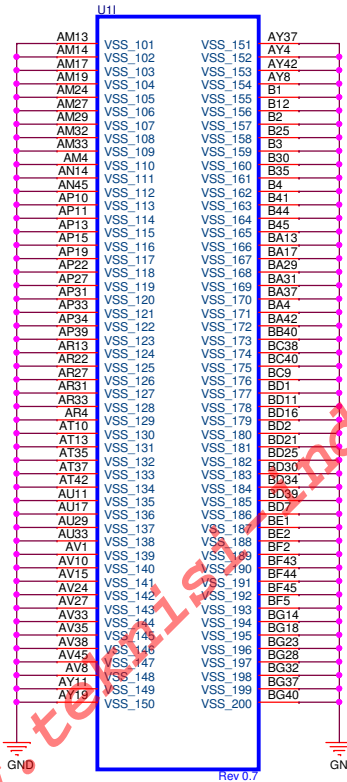
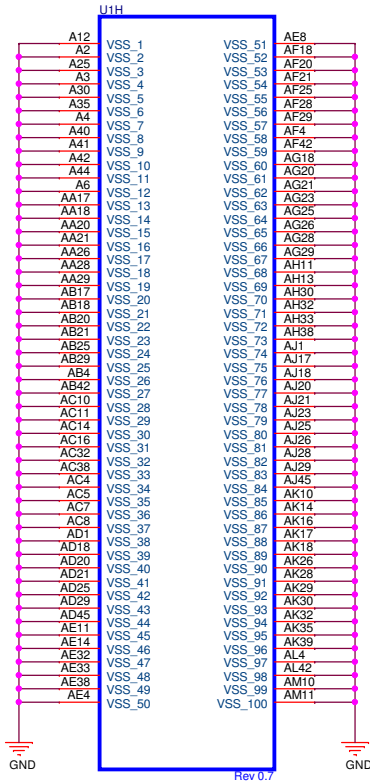
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Size A3	Project Name MFF	Rev A00
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Date: Sheet 22 of 97

KABYLAK_PCH





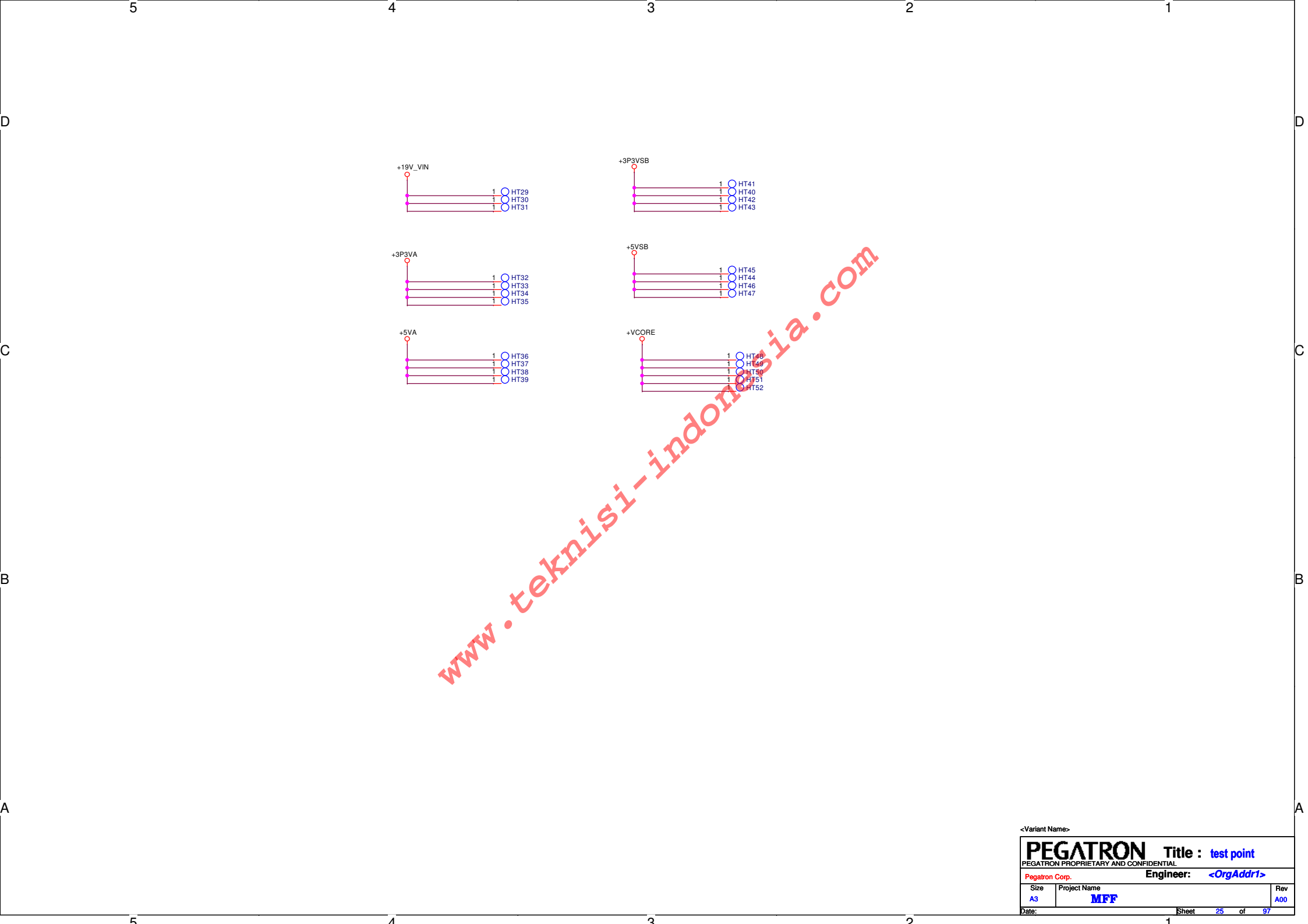
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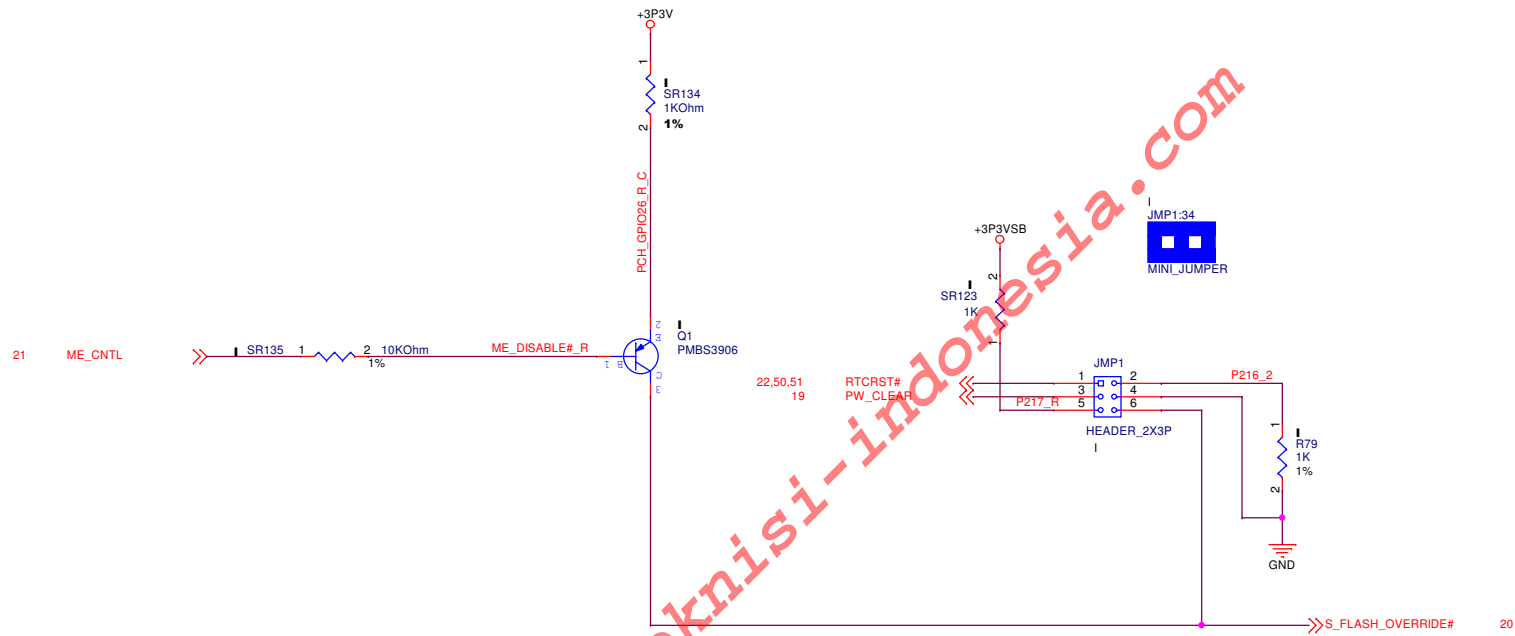
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PEGATRON PROPRIETARY AND CONFIDENTIAL

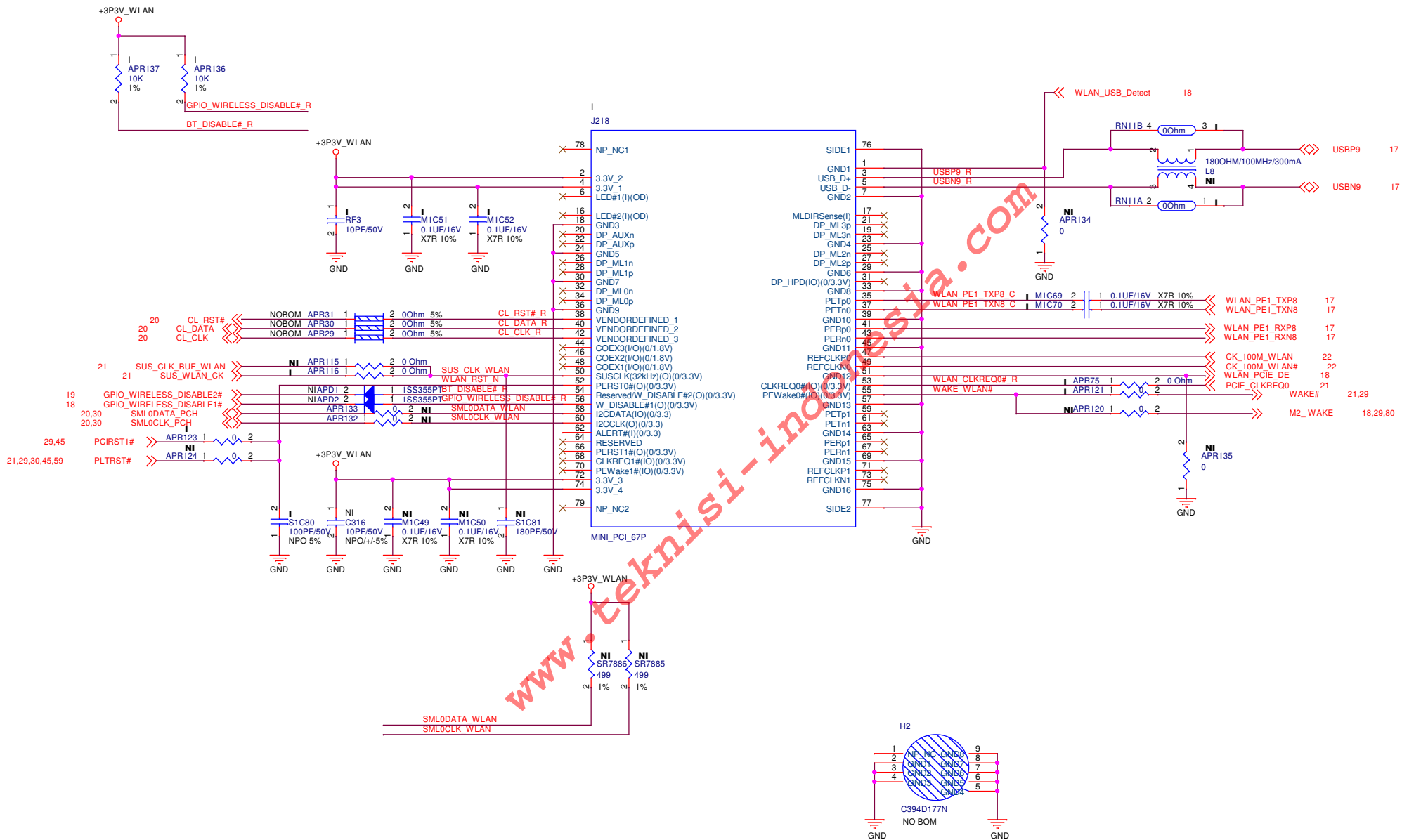
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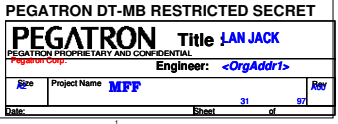
Size	Project Name	Rev
A3	MFF	A00

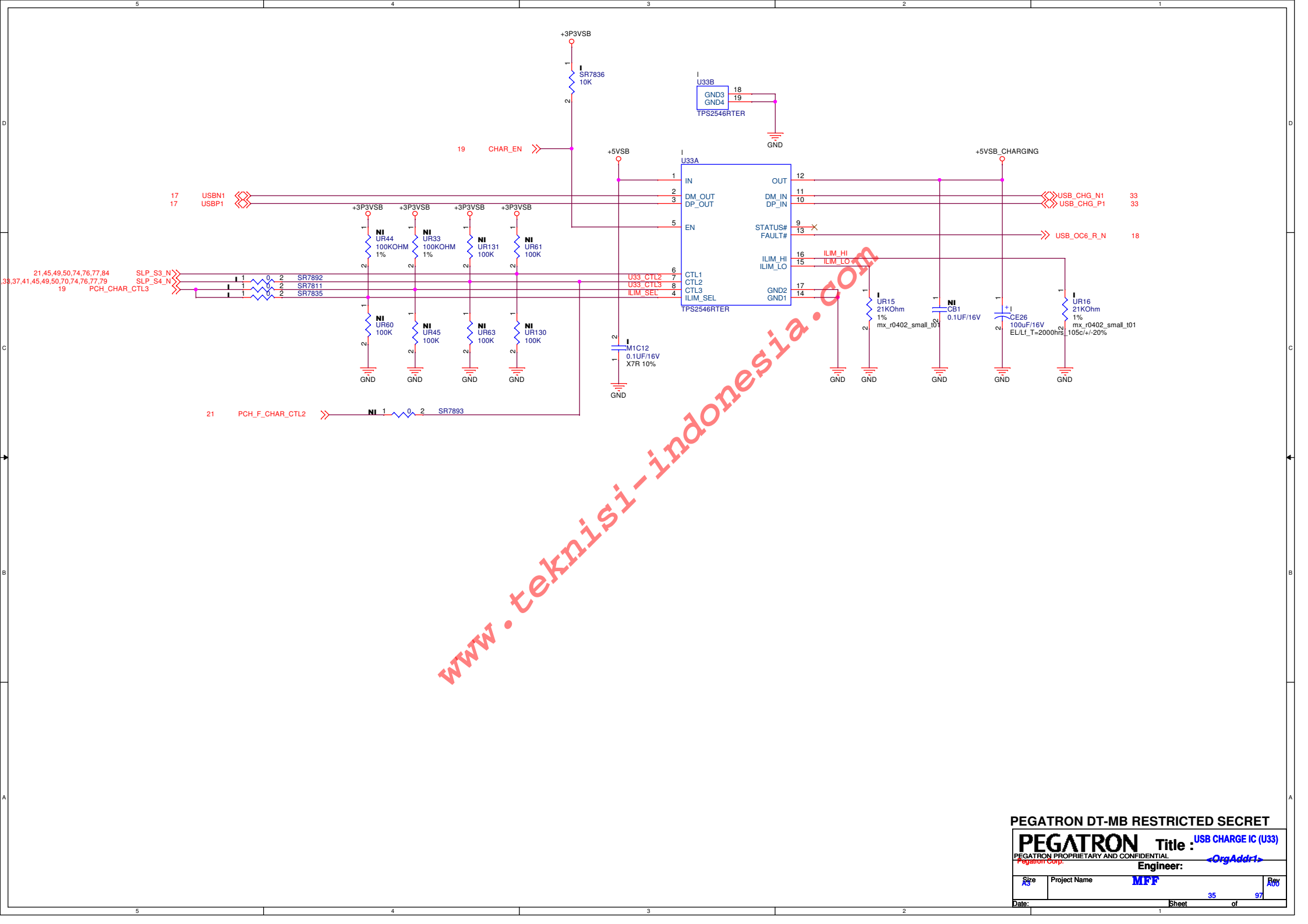
Date: Sheet 24 of 97









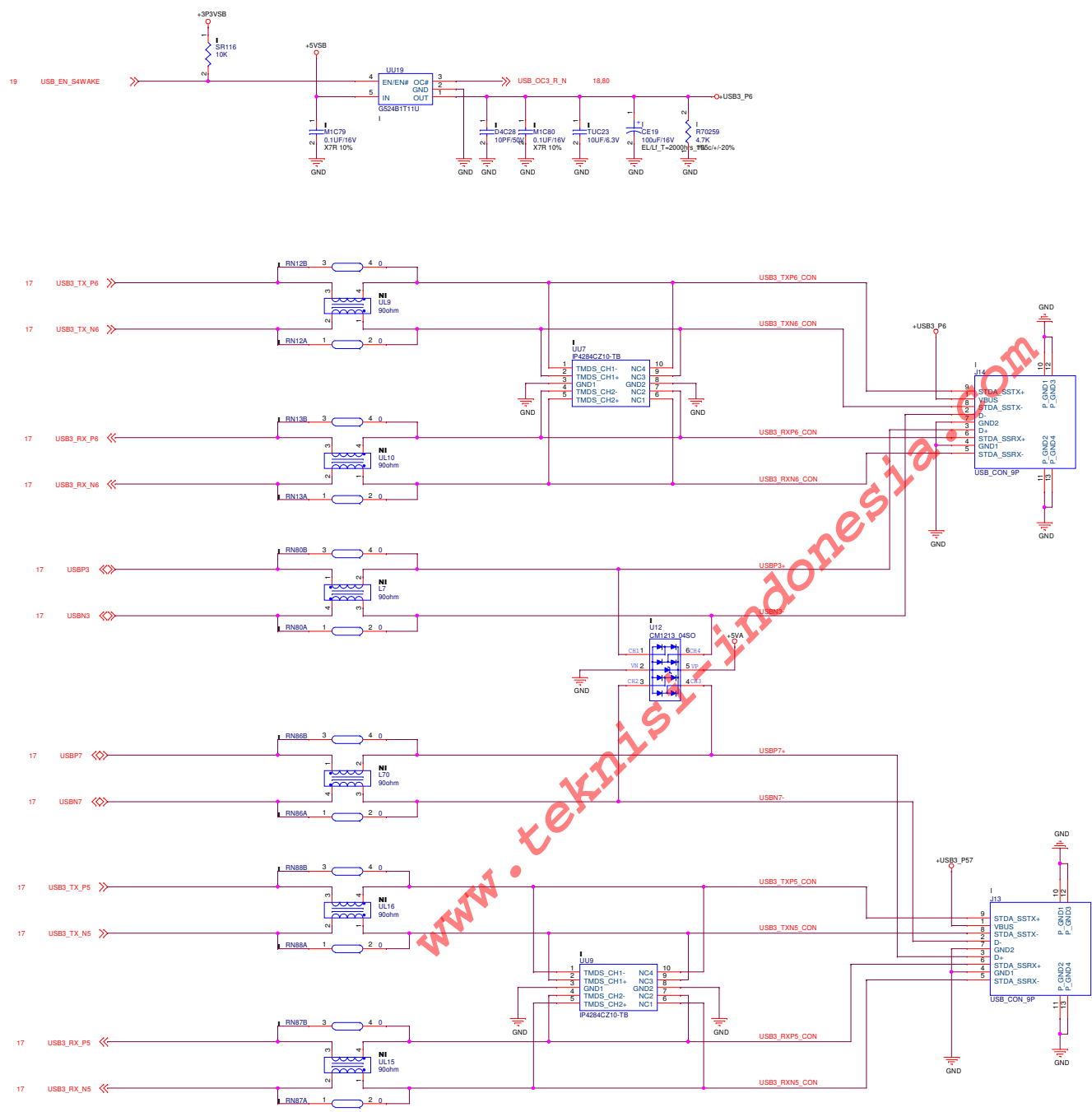


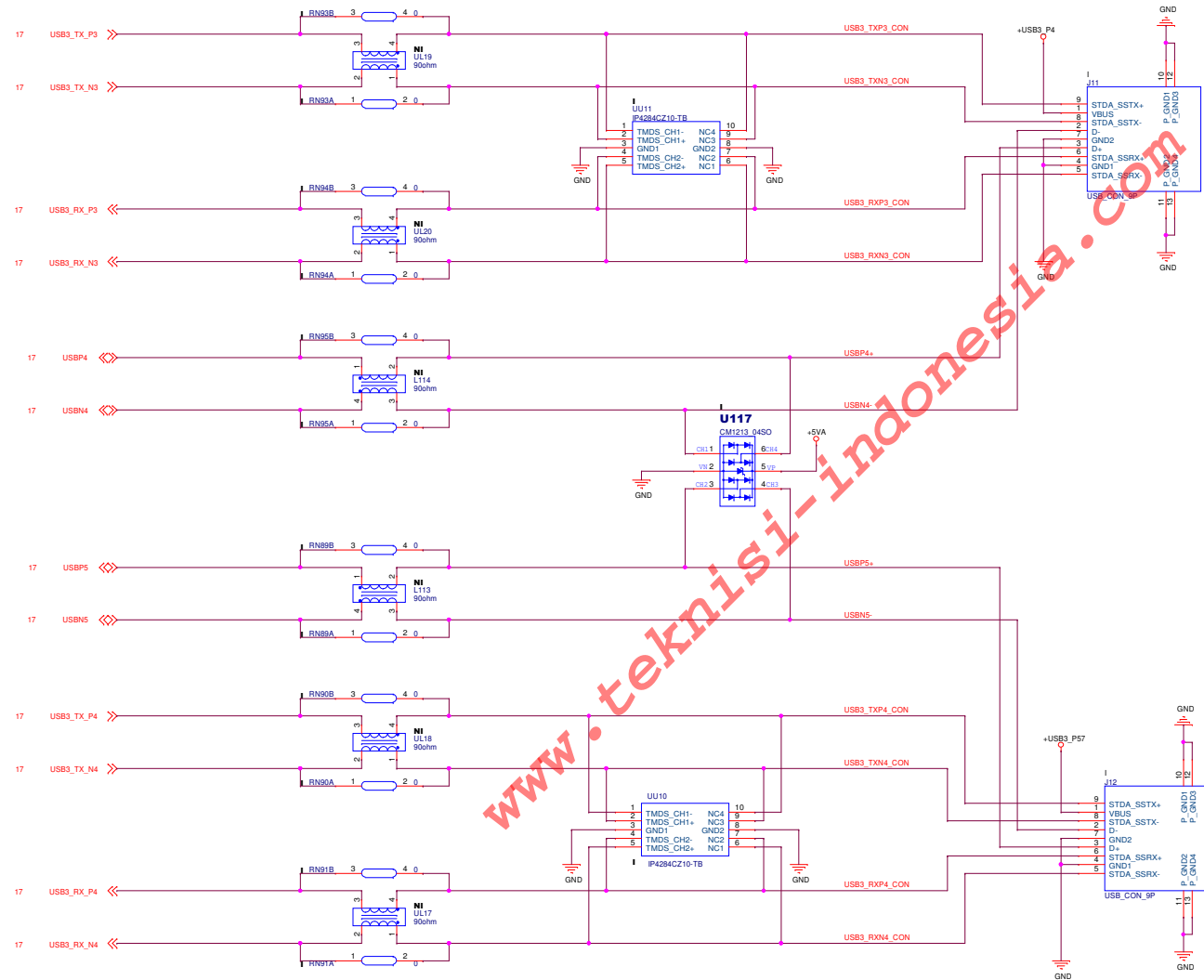
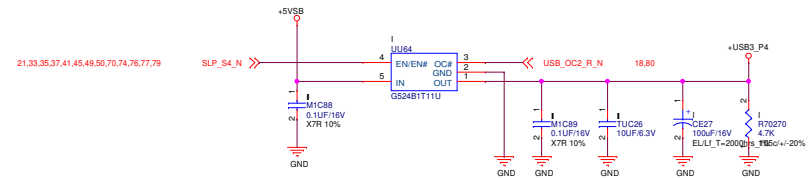
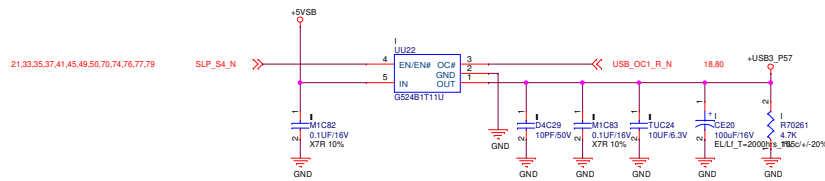
PEGATRON DT-MB RESTRICTED SECRET

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Pegatron Corp. Engineer: <OrgAddr1>

Size	Project Name	Rev
35	MFF	97

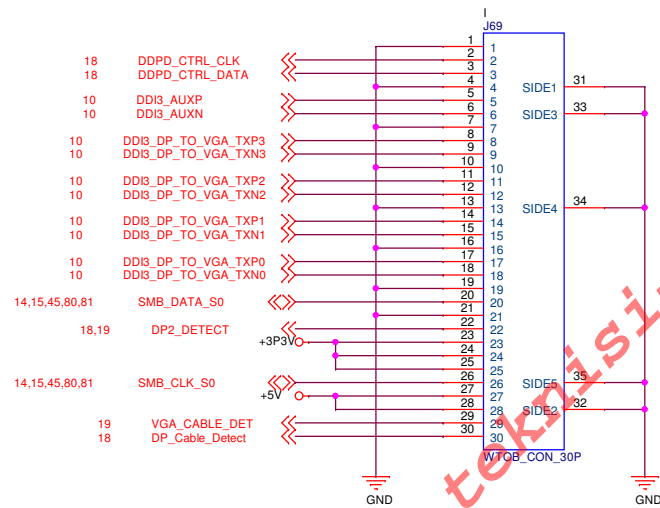
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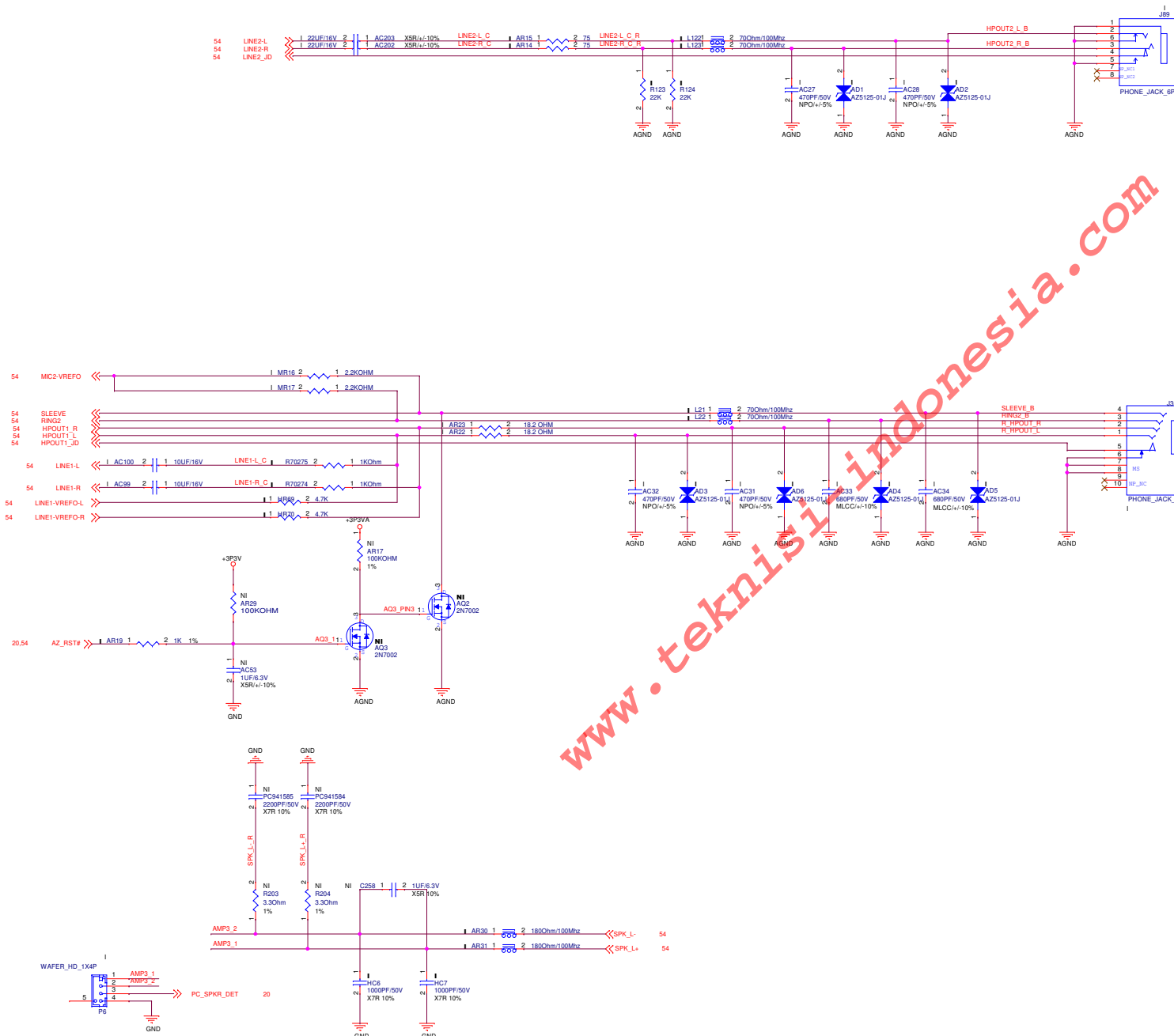
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Size	Project Name	MFF	Rev
Umk	Sheet	37	37



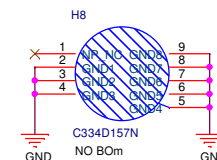
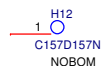
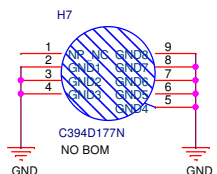
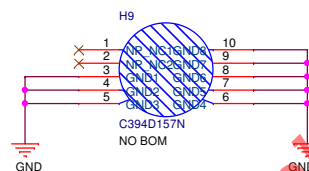
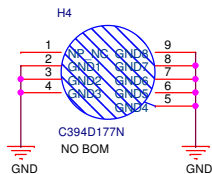
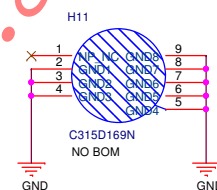
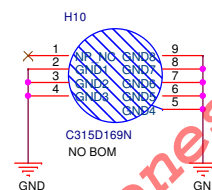
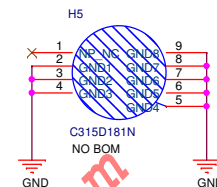
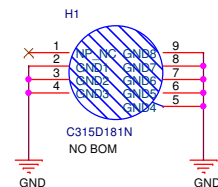
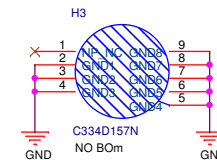
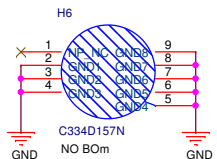
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Pegatron Corp.		Engineer:	
Size	Project Name	Rev	Rev
42	MFF	42	97
Date:	Sheet of		



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PEGATRON DT-MB RESTRICTED SECRET

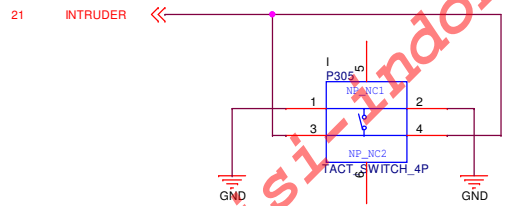
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PEGATRON PROPRIETARY AND CONFIDENTIAL

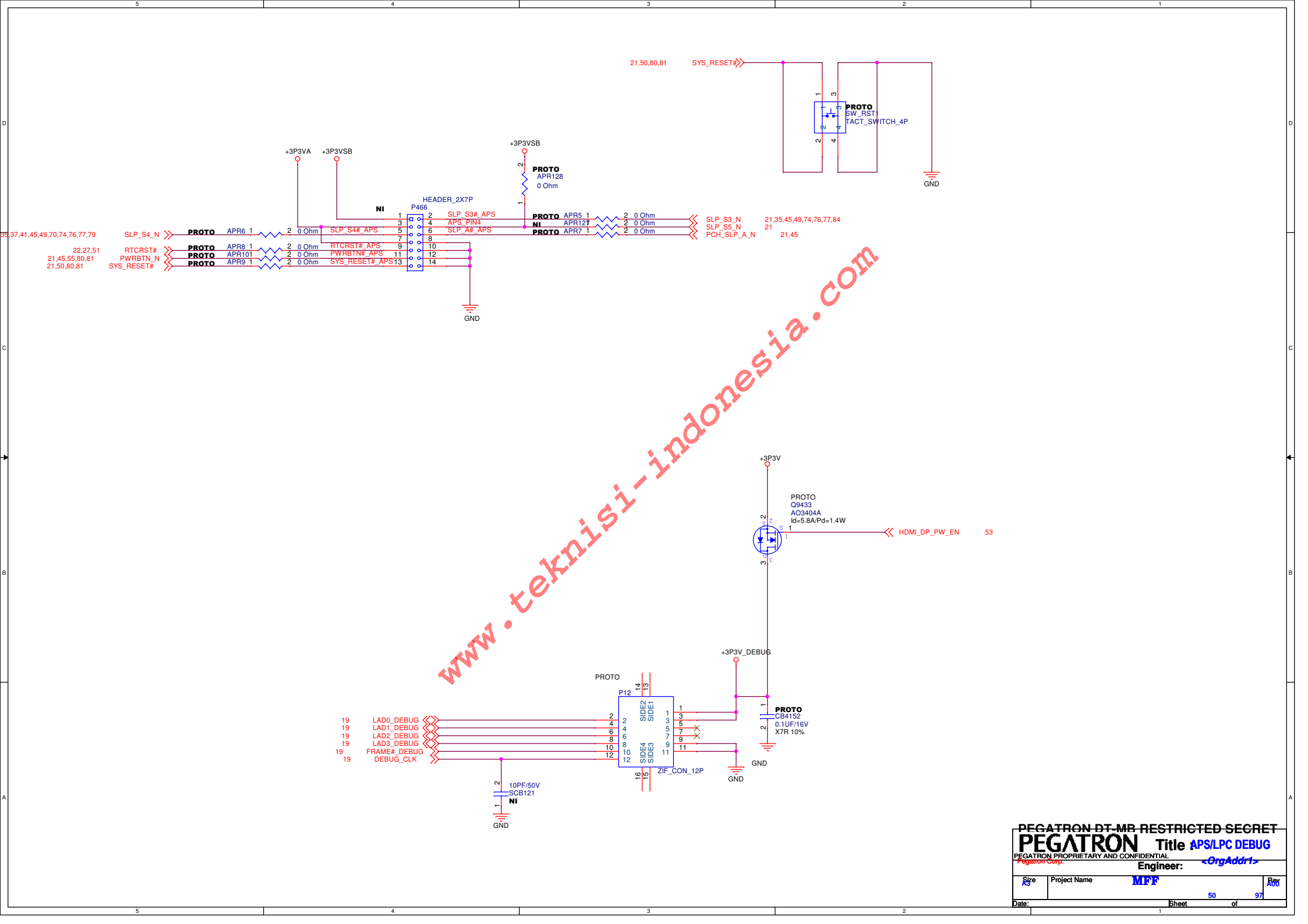
Engineer: <OrgAddr1>

Pegatron Corp.
Size A3 Project Name MFF

Date: Sheet 46 of 97

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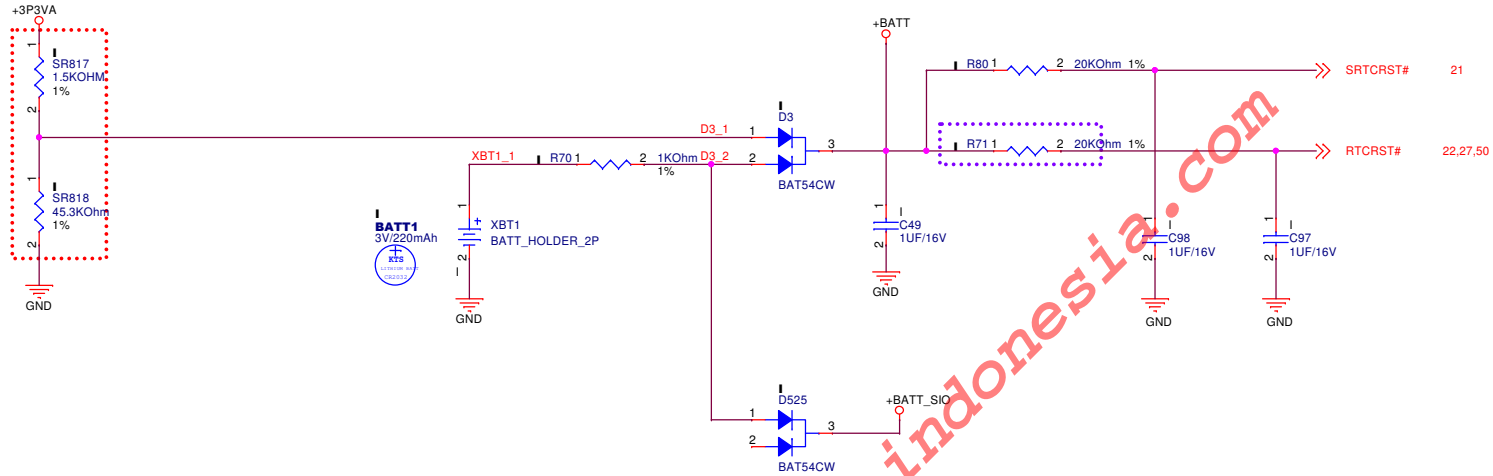


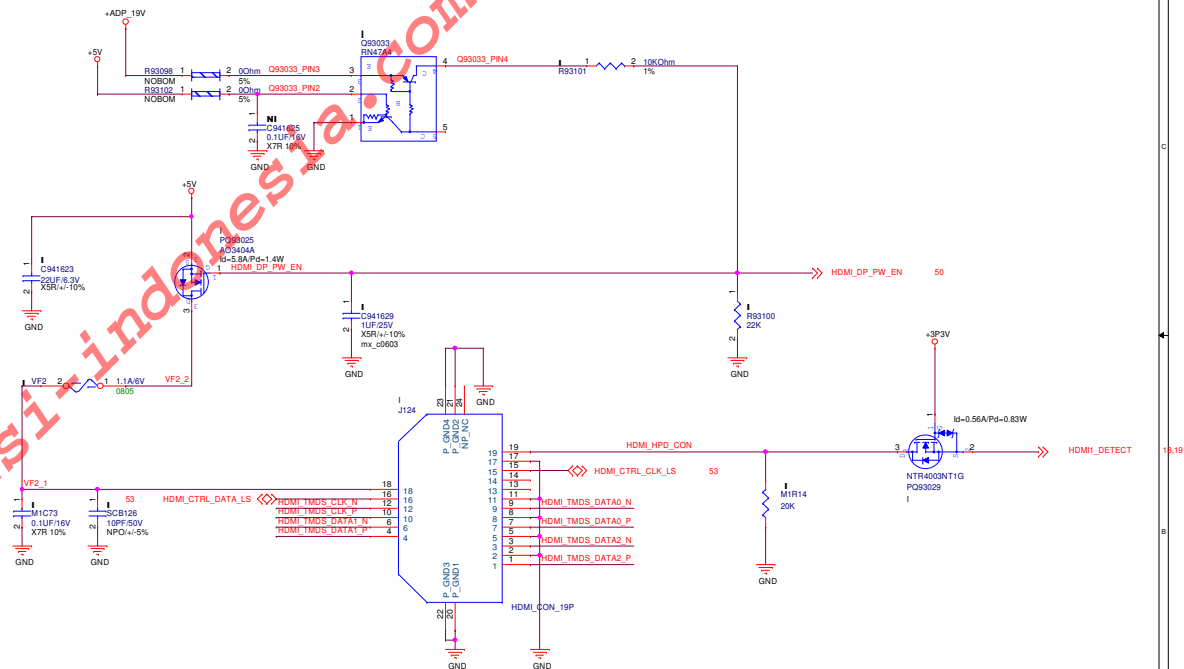


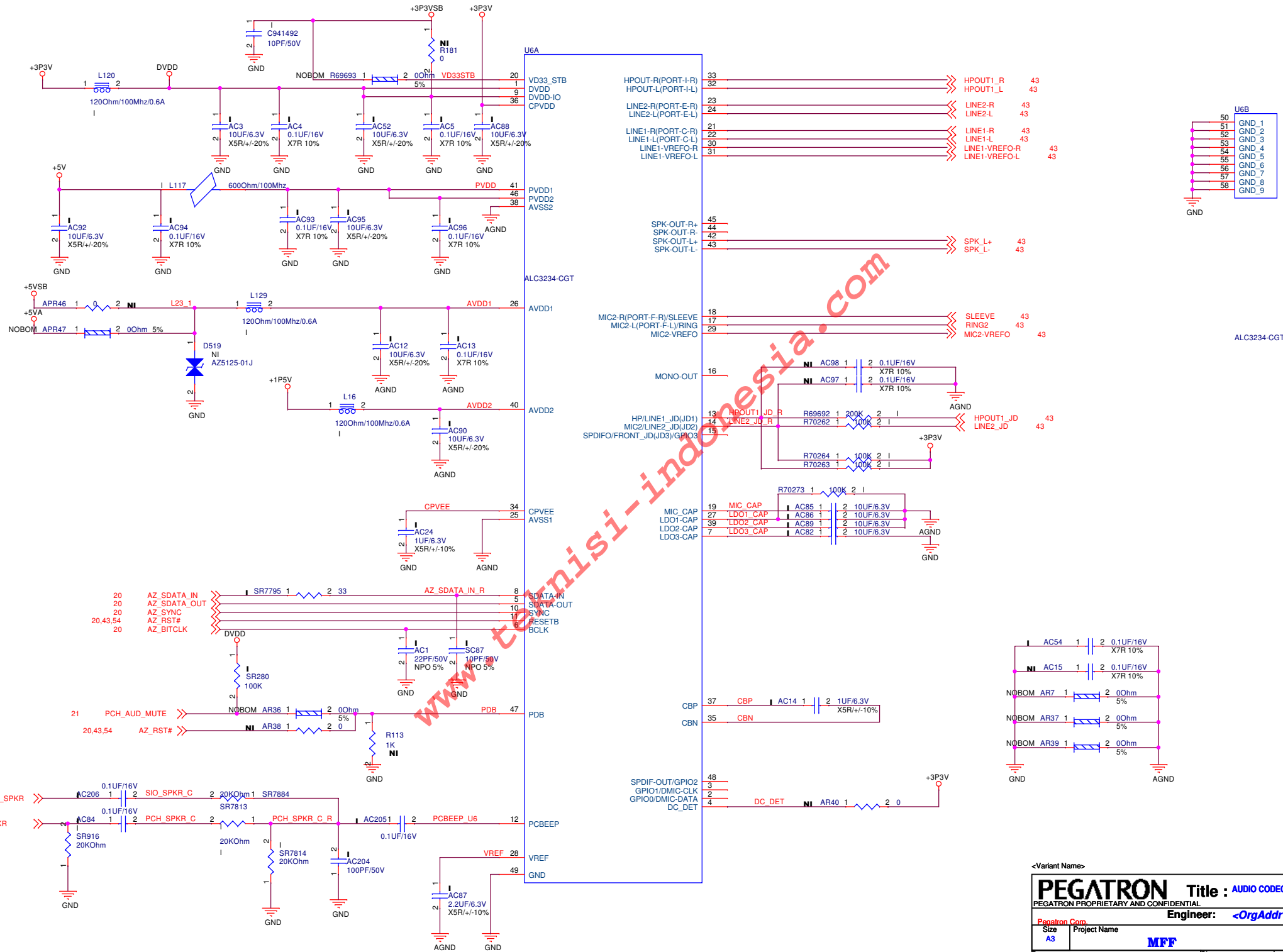
1103 by PDG p324
VCCDSW 3p3 to drop the voltage and meet the max
VCCRTC < 3.2V specification. The cost impact is small but
this solution will result in an ~0.25 mW power loss in
non-G3 state. In this solution, the dual diodes must be in a
single Si package to ensure matched Vf characteristics.
Initial resistor value recommendations are R2=1.5 KΩ and
R3=45 KΩ.

RTC

Original circuit design 27.4K(10X212274310)
Intel Sequence asked 20K 1%, CRB asked 30.1K.







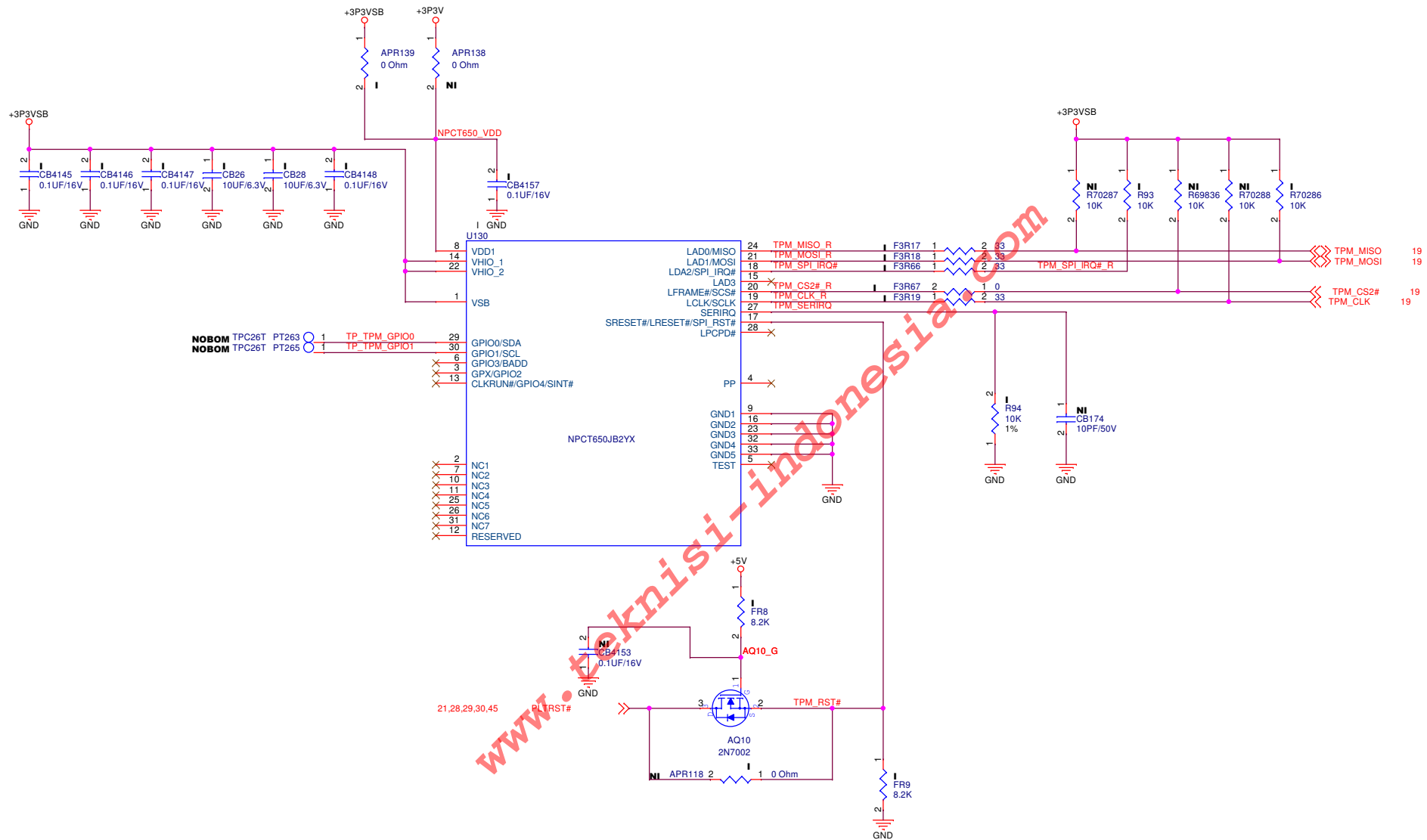
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PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: <OrgAddr1>

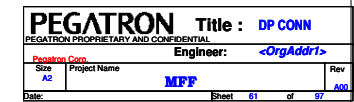
Size A3	Project Name MFF	Rev A00
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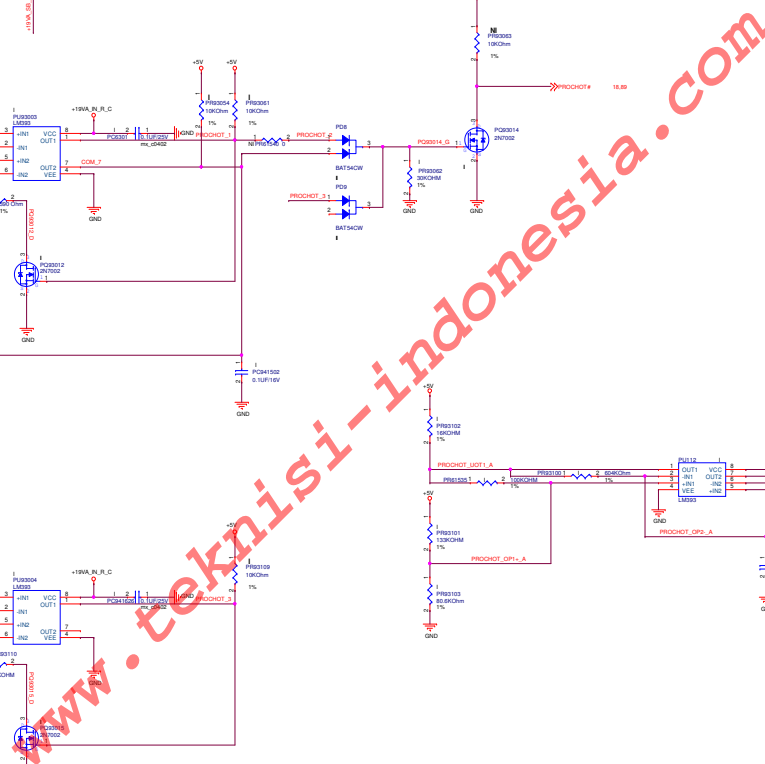
Date: Sheet 54 of 97

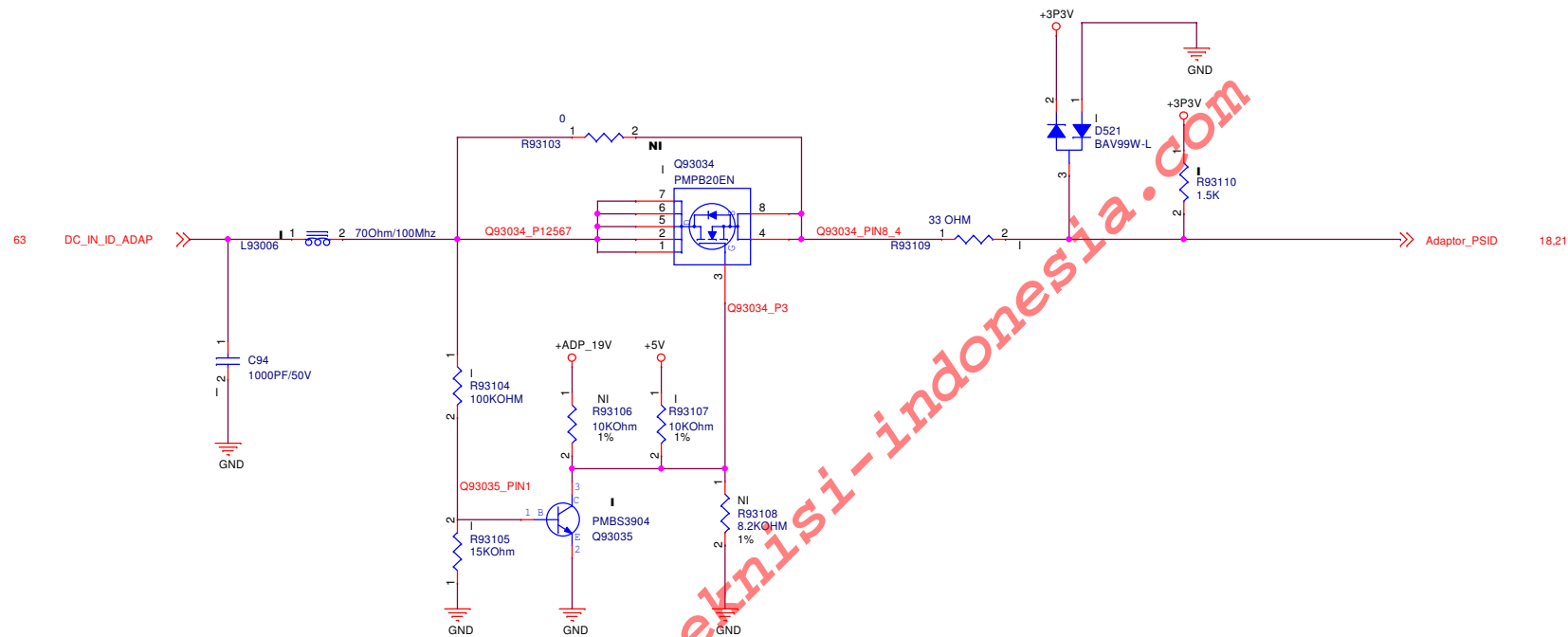


PEGATRON DT-MB RESTRICTED SECRET

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Size	Project Name	Rev	
A3	MFF	A00	
Date:	Sheet 59 of 97		

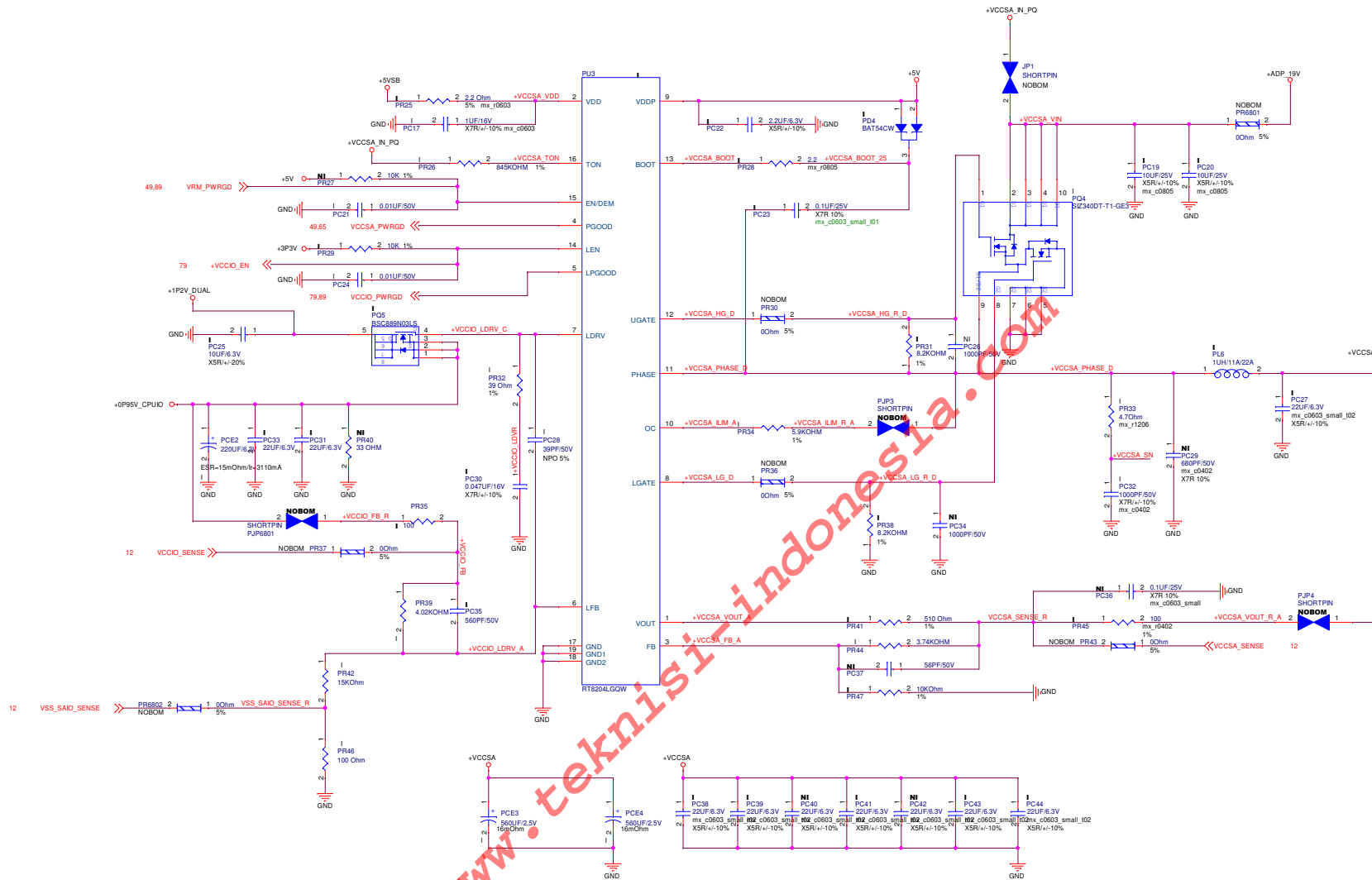


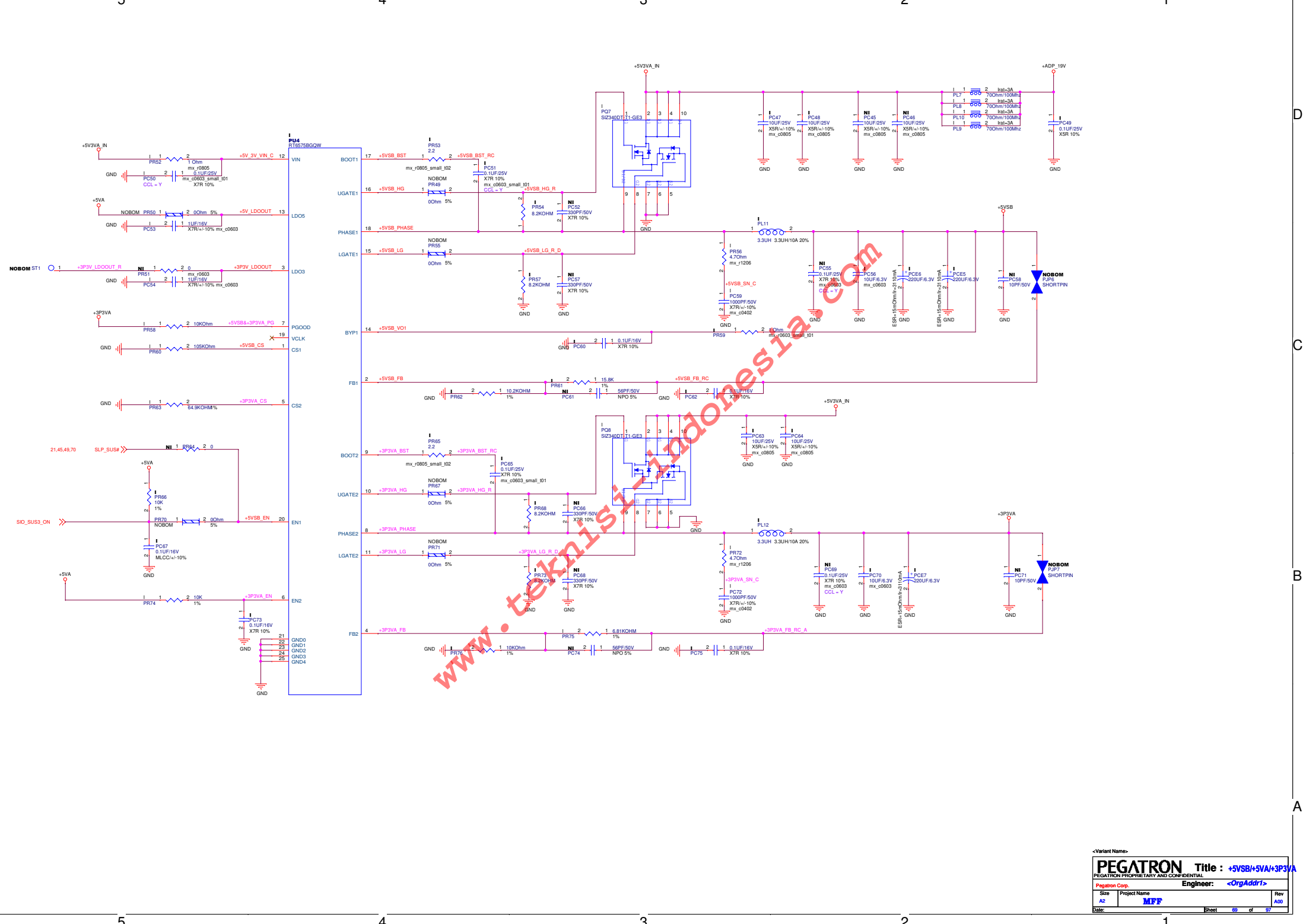


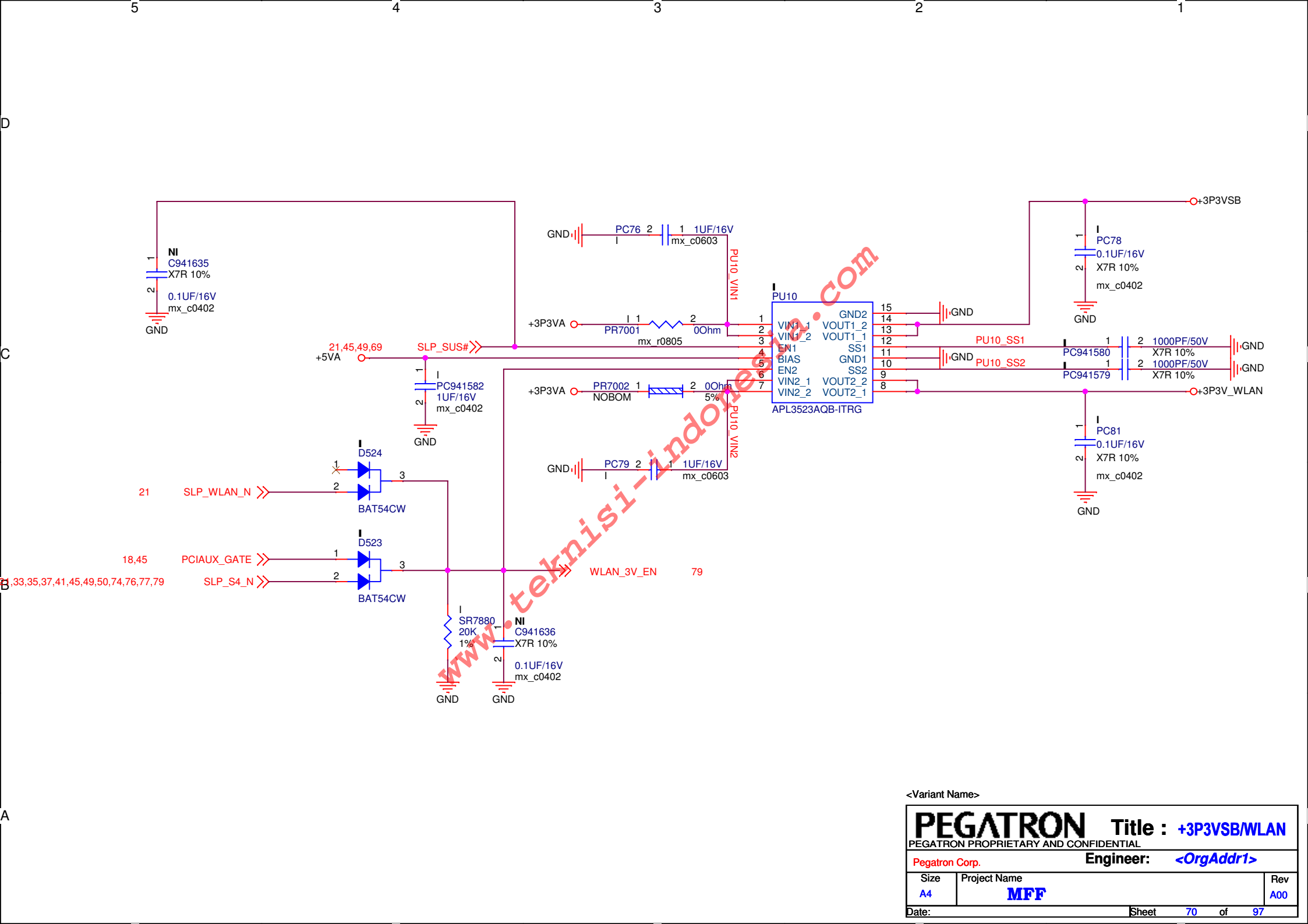


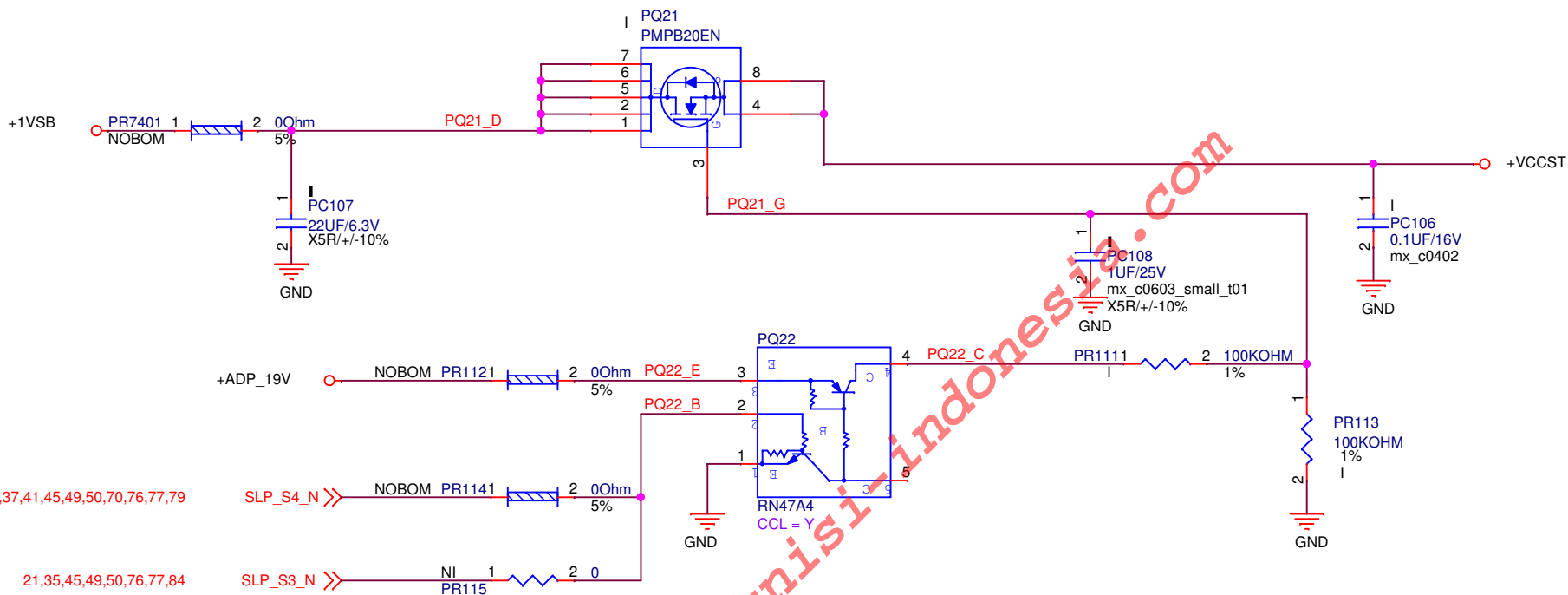
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Size A3	Project Name MFF		Rev A00
Date:	Sheet 64 of 97		



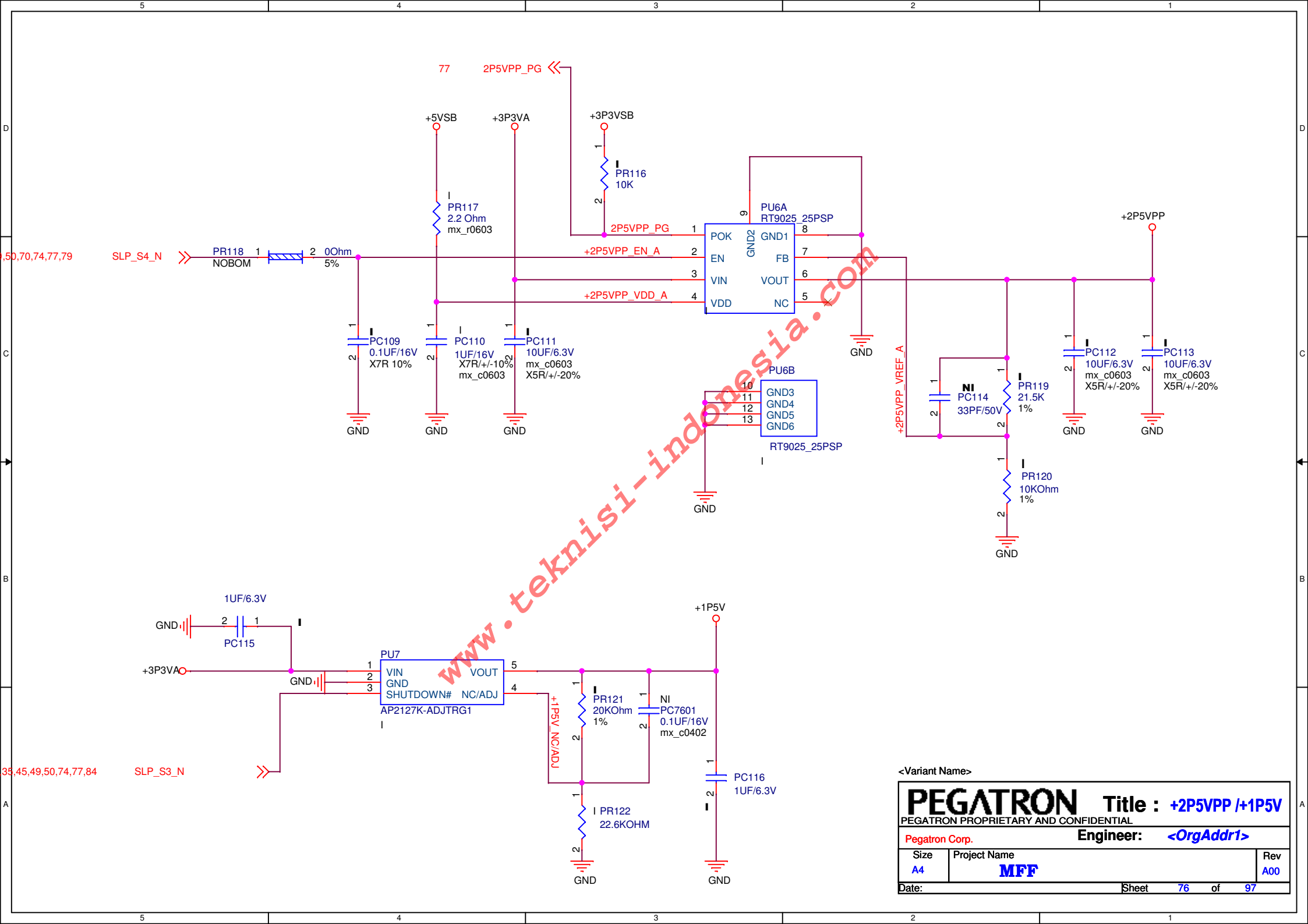






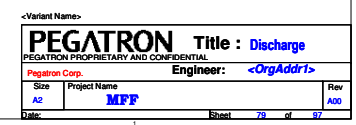
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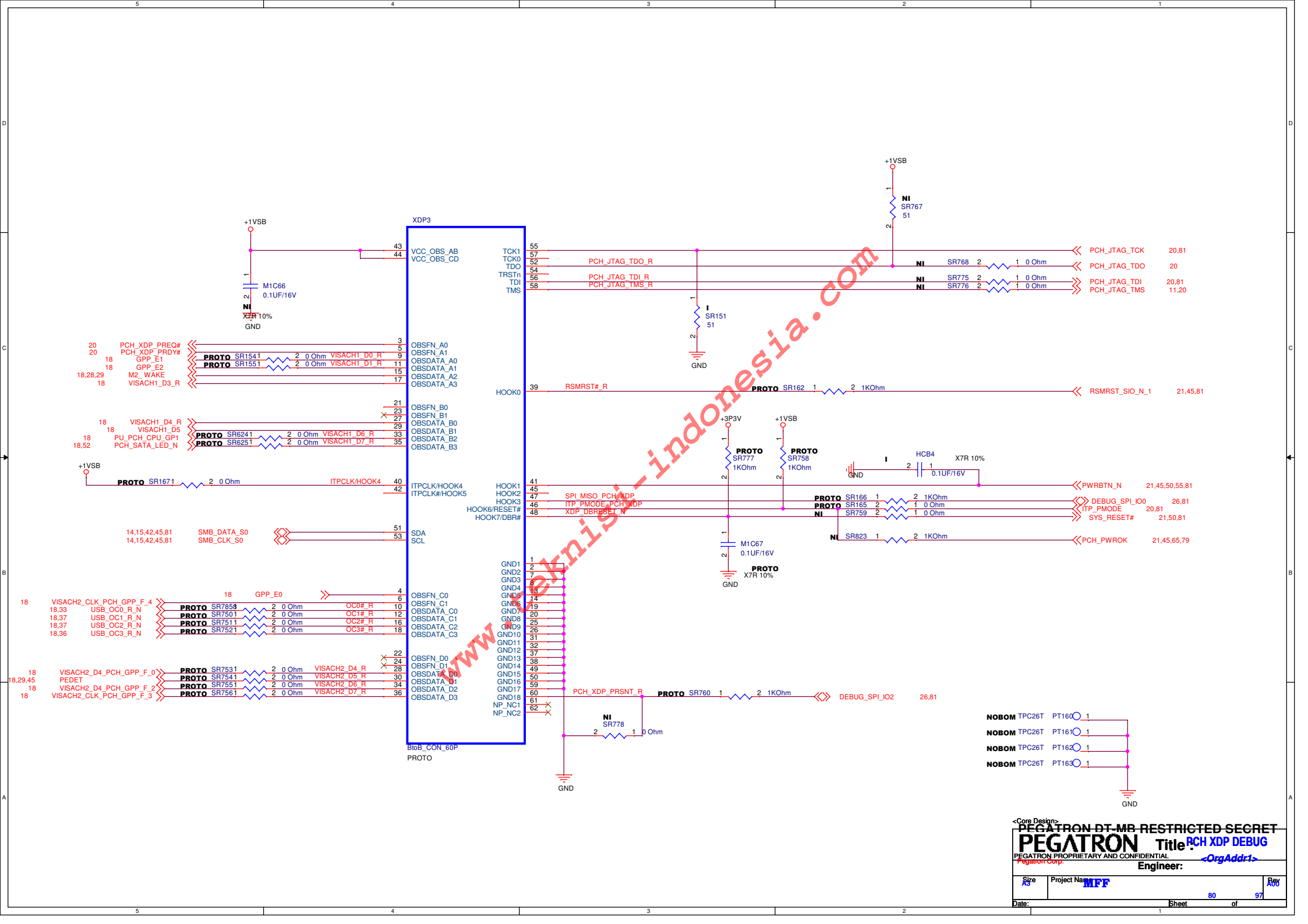
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
Pegatron Corp.		Engineer: <OrgAddr1>	
Size A4	Project Name MFF		Rev A00
Date:		Sheet 74 of 97	

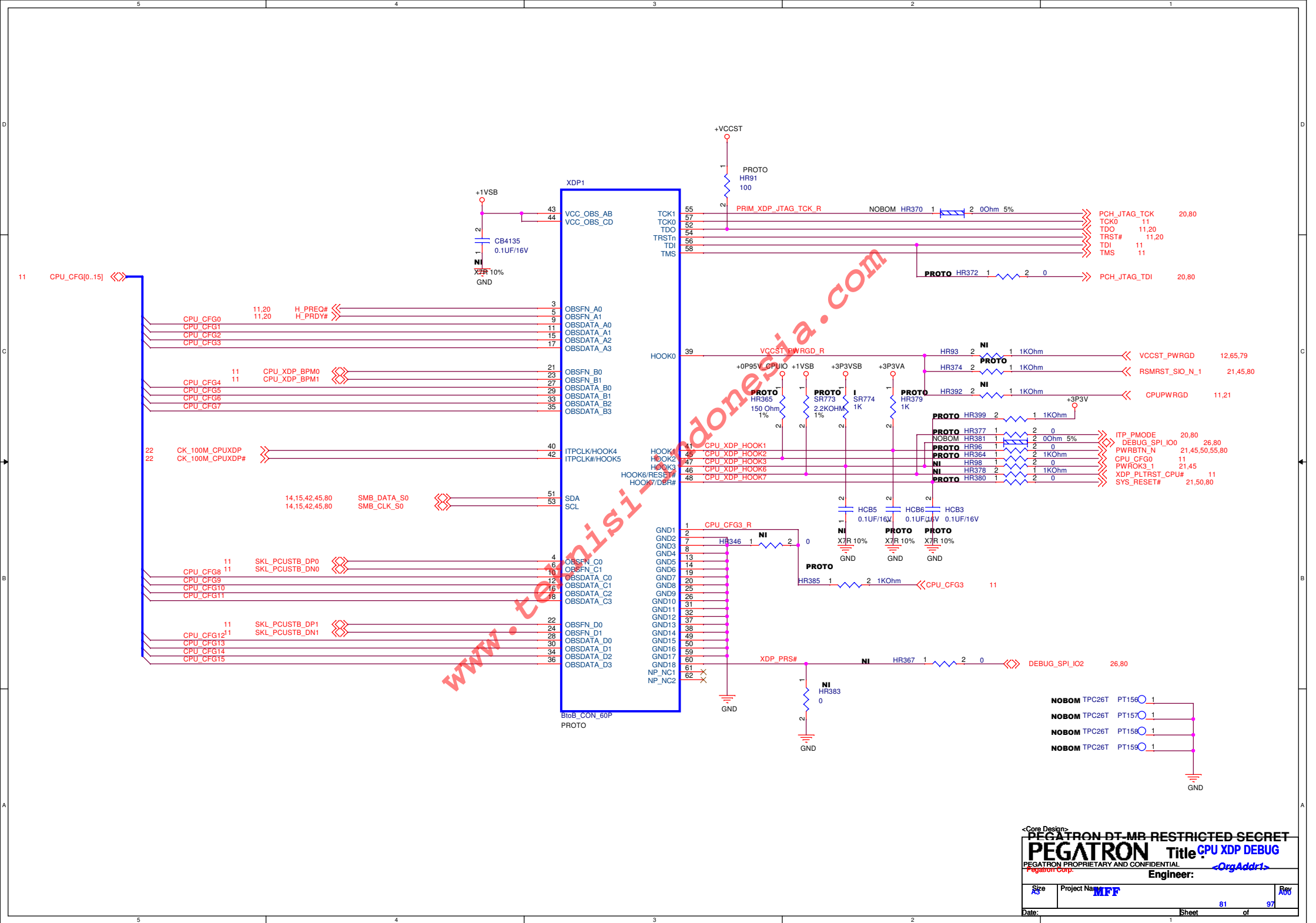


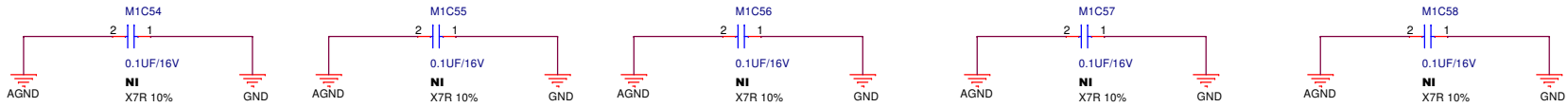
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
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Size A4	Project Name MFF		Rev A00
Date:		Sheet 76 of 97	

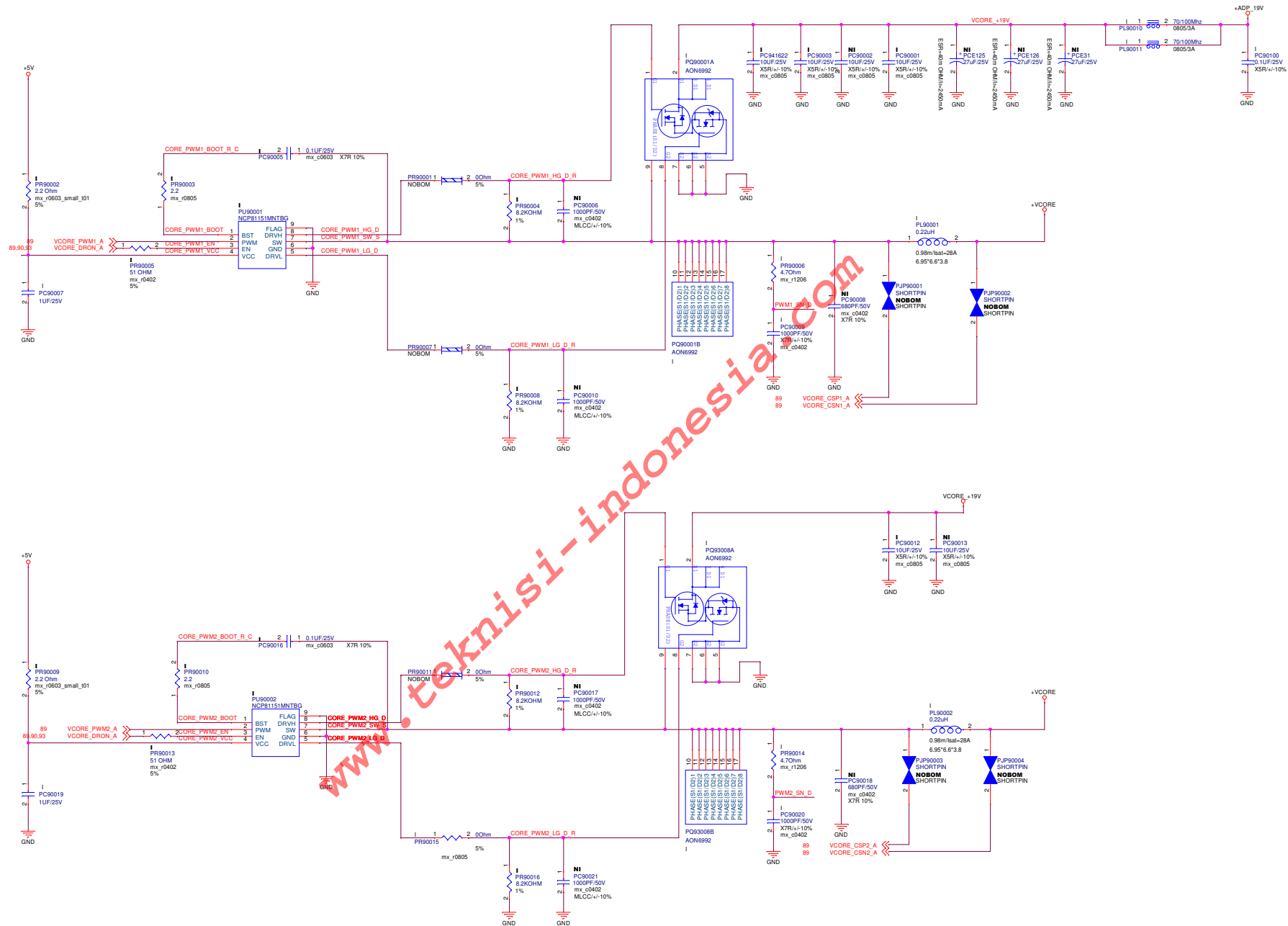


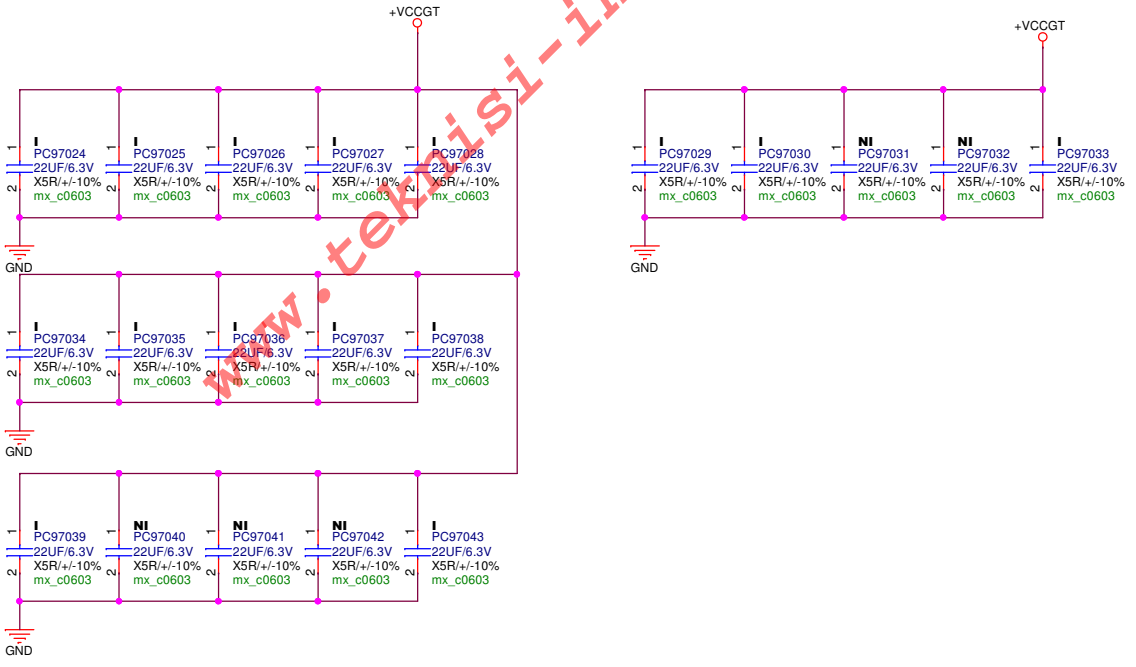
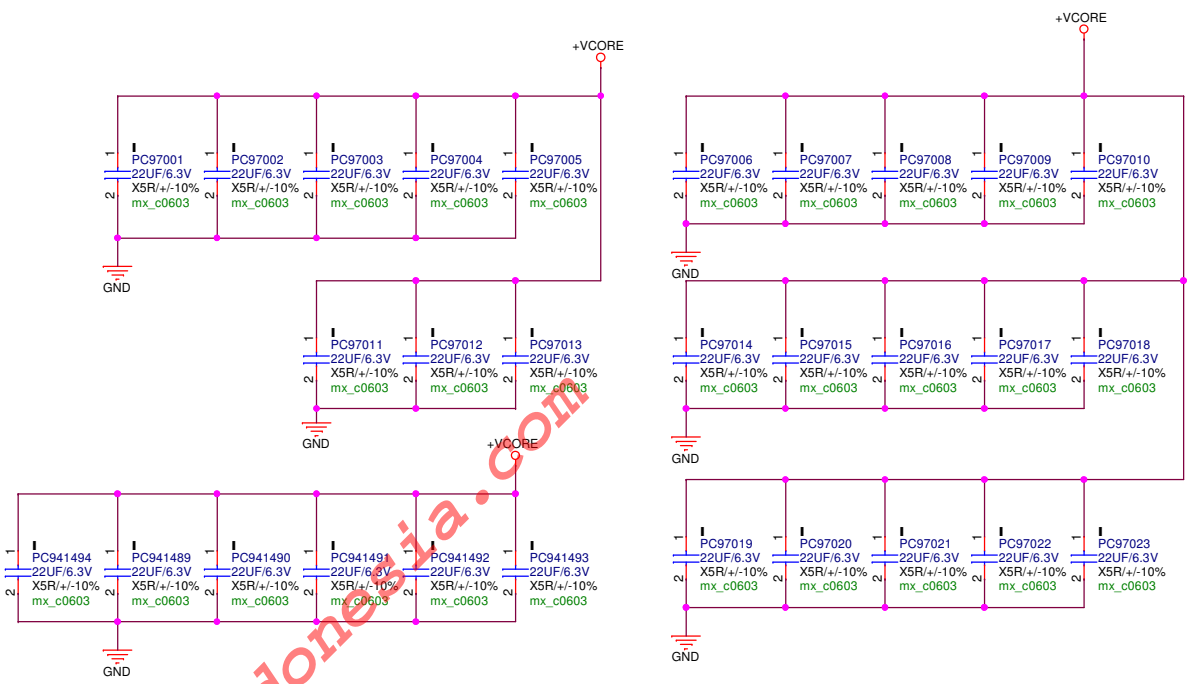
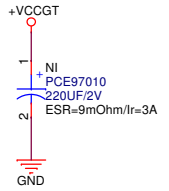
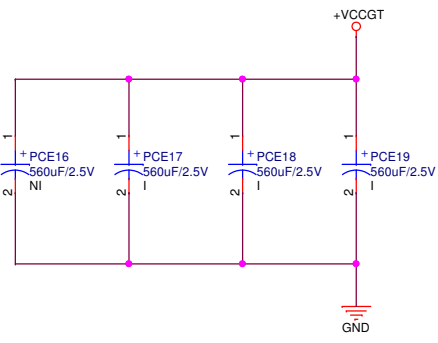
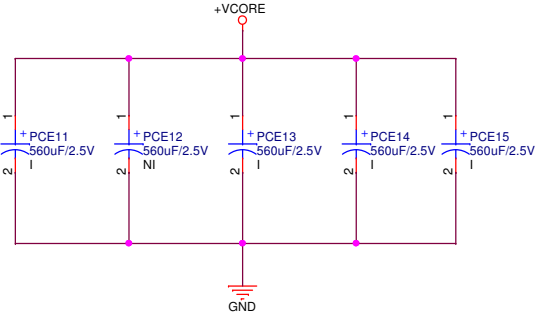






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<Variant Name>

PEGATRON Title : CORE & VCC_GT CAP	
PEGATRON PROPRIETARY AND CONFIDENTIAL	
Engineer: <OrgAddr>	
Size	Project Name
Custom	MFF
Date:	Sheet 97 of 97